

## PLL and DLL Hard Macros

True Circuits' complete family of standardized, silicon-proven, low-jitter PLL and DLL hard macros spans nearly all performance points and features typically requested by ASIC, FPGA and SoC designers. Using robust state of the art circuits, a methodical and proven design strategy, and close associations with the world's leading fabs, IDMs and design services companies, True Circuits is able to quickly and reliably create new and innovative designs in a variety of advanced process technologies.

True Circuits' clock generator, spread spectrum, low bandwidth and deskew PLLs support wide operating frequency ranges and multiplication factors over which they deliver optimal performance, avoiding the cost and complexity of licensing multiple point-solution PLLs from other vendors. The clock generator PLL is available with multi-phase outputs. The spread spectrum PLL allows precise adjustment of spreading rate and depth, with 4 bits of precise fractional-N control, optional multi-phase outputs, and very low long-term jitter. All PLLs are available in small sizes for easier integration.

True Circuits' DLLs delay a set of signals by precise and adjustable fractions of a reference clock cycle independent of voltage and temperature. These DLLs are available in mutli-slave and multi-phase versions, have flexible form factors for easier integration and are ideal for high-speed DDR and other interface applications.

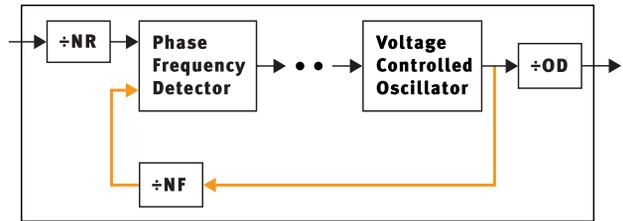
True Circuits' high-quality, low-jitter, silicon-proven timing hard macros are available for immediate delivery in a range of frequencies, multiplication factors, sizes and functions in TSMC, GlobalFoundries, UMC and Common Platform processes from 180nm to 28nm. Customized solutions are also available for specialized chip applications.

DAC Booth #1356

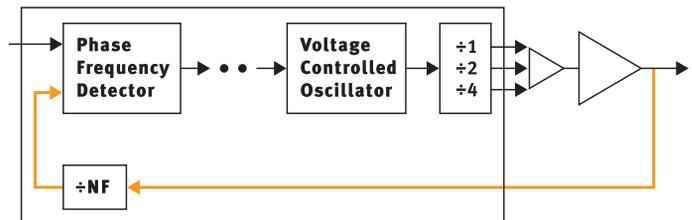
### FEATURES & BENEFITS

- ◆ Clock Generator, Spread Spectrum, Low Bandwidth and Deskew PLLs
- ◆ High-speed DLLs
- ◆ Support the latest DDR, SerDes, video and audio standards
- ◆ Low-jitter and very process tolerant
- ◆ Large multiplication factors (1-4096)
- ◆ Wide output frequency ranges
- ◆ Small sizes and flexible form factors
- ◆ Pin Programmable

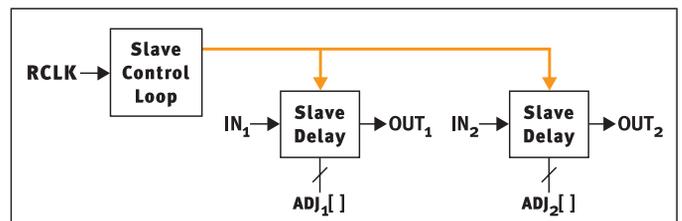
CLOCK GENERATOR, SPREAD SPECTRUM, LOW BANDWIDTH AND HIGH RESOLUTION PLLS



DESKEW PLL



DDR DLL



### DELIVERABLES

- ◆ Available in TSMC, GlobalFoundries, UMC and Common Platform processes from 180nm to 28nm
- ◆ GDSII and LVS Spice netlists
- ◆ Behavioral, synthesis and LEF models
- ◆ Extensive user documentation
- ◆ Integration support to ensure successful tape outs

### CONTACT INFORMATION

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