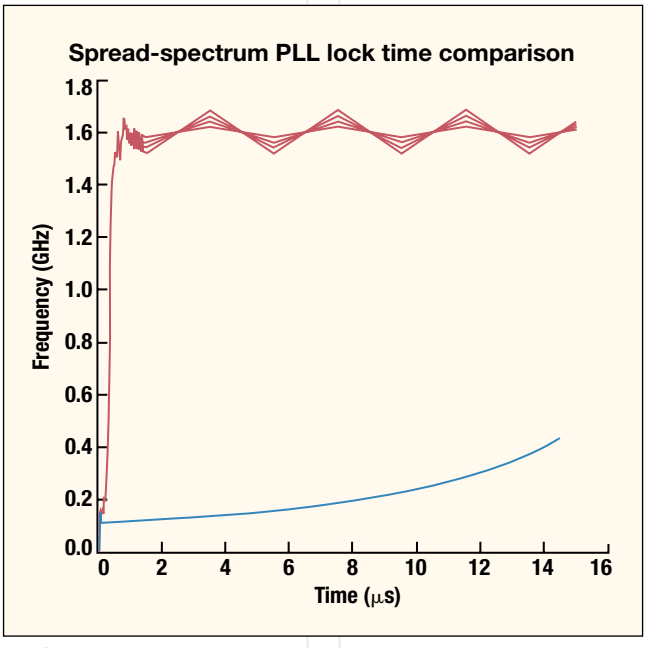
PLLs Plot An Adjustable Course

BY CHERYL AJLUNI

This Line Of Phase-Locked-Loop Analog Hard Macros Allows Wireless Engineers To Automatically And Precisely Dial In On Both Bandwidth And Spectrum.

PHASE-LOCKED loops (PLLs) are commonplace in applications like cellular phones, wireless transceivers, and Global Positioning Systems. Despite their familiarity to systems engineers, however, PLLs come with their own unique set of challenges. For instance, they inherently take a long time to lock. Techniques can be employed to help them lock quickly. But those techniques give up performance to provide what they can in locking capability. Such techniques must therefore be conservative in the way that they allow the PLL to lock. They require an extra amount of control to be added to a design. In addition, the techniques can cause a PLL to miss the target frequency by some given amount—a problem often referred to as "overshoot." These problems put wireless applications in an unenviable position, as they are driven by low-power, high-performance operation. Low-power constraints demand that PLLs be turned off during inactivity, but then require that they lock quickly when turned back on.

Recognizing this dilemma, True Circuits set out to develop PLLs that could eliminate these concerns. Ideally, the resulting PLLs would not require any external controls. And in an innovative twist, they also would leverage the concept of self-biasing in the solution. The result of this effort culminated in two separate phase-locked loops: the Low-Bandwidth PLL and the Spread-Spectrum PLL.



1. Output frequency is plotted as a function of time after reset. The top curves, with fast-locking circuitry enabled, lock very quickly. In contrast, the bottom curve, with circuitry disabled, does not reach lock in the allotted time.

Both of these PLLs flaunt unique functionality. They boast low jitter and special circuitry that is referred to as LockNow! Technology. This technology enables very fast locking without adding frequency overshoot. The result is an improvement in PLL lock times by two or more orders of magnitude with the same level of input-period jitter rejection as before. That's roughly equivalent to less than 1000 output cycles, mostly independent of bandwidth and multiplication factor. (Don't confuse output cycles with reference cycles, as each reference cycle contains multiple output cycles.)

John Maneatis, True Circuits' President, explains it this way: "Circuit designers need flexibility in implementing third-party intellectual property (IP). These new PLL designs were developed so designers could make adjustments to the PLLs during integration without being held to a rigid specification. The adjustment settings that they feature are not a mechanism to tweak the designs so that they work. Rather, they allow a small set of designs to satisfy a large set of applications. Uniquely, these designs are very process and environmentally insensitive."

Core to the PLL analog hard macros is True Circuit's LockNow! technology **(FIG. 1)**. This technology allows the PLLs to achieve lock in essentially constant time at a particular output fre-

quency. This occurs independently of the feedback divider and bandwidth settings and regardless of the loop bandwidth for a given output frequency. Plus, it adds no additional frequency overshoot.

This fast-locking capability affords the True Circuits' PLLs a big advantage. They can now multiply the clock by a large number or operate at a reduced bandwidth. In both cases, the net effect of reducing bandwidth has typically lead to an increase in clock lock time. With True Circuits' PLLs, though, special circuitry was added. It substantially boosts the bandwidth during locking without causing overshoot. This technology allows the circuit to be turned on when needed and then automatically shut off when not in use. In portable devices, the result is a drastic cut in power consumption.

In addition to the LockNow! Technology, both PLLs offer a host of innovative capabilities. The low-jitter Spread-Spectrum PLL boasts an adjustable bandwidth, spreading rate, and spreading amount. The spreading function is included in the ASIC—a move that significantly reduces manufacturing costs. The Spread-Spectrum PLL is designed to multiply an input clock by an integer or fixed-point number. Its frequency-spreading capability is suitable for applications requiring spread-spectrum clock sources to satisfy FCC requirements for RF emissions **(FIG. 2)**.

Traditionally, it has been difficult to control the PLL spreading amount with a particular setting. The circuitry has simply been unable to comprehend the idea of downspreading only, which is important for applications where the maximum frequency is a hard specification. Without control over the exact amount of spreading that takes place, the PLLs can be difficult to use. In contrast, the True Circuits' Spread-Spectrum PLL employs circuitry that eliminates variability in the actual spreading amounts. The PLL generates a spread-spectrum clock, as the clock frequency typically varies in a sawtooth pattern over time. As a result, it can precisely target and hit a specific maximum output frequency for a given spreading amount. This reduces EMI emissions from chips. The amount of the reduction depends heavily on the application in question.

Yet this capability does have one drawback: increased jitter (typically up to 2%) from the PLL. By watching this parameter closely, however, the engineers who are using the PLL can successfully limit any increase. To aid the engineer in this task, True Circuits built in adjustment points. When the spreading capability is turned off, the period jitter performance is on the order of 2% peak to peak.

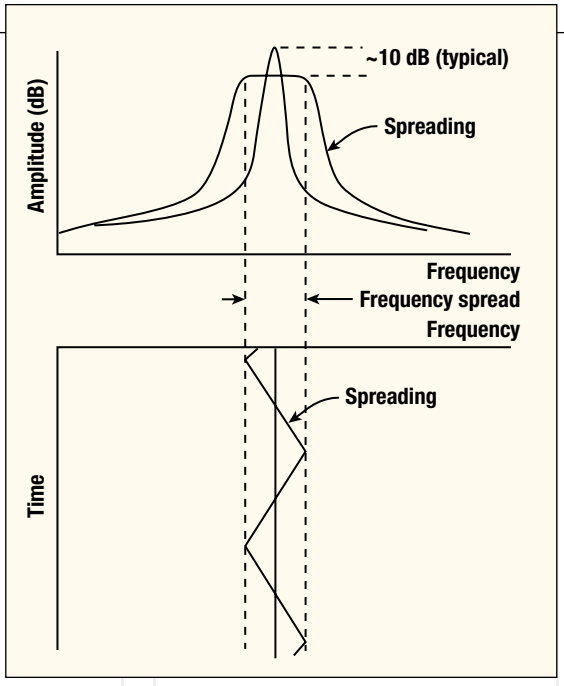
The company's other PLL offering—the Low-Bandwidth PLL—was designed to address the excessive jitter from system clocks. It generates high-speed clocks, which are often required for processors and chip interfaces with low-jitter performance. For example, say an engineer is working with a poor-quality clock or needs a cleaner signal. The Low-Bandwidth PLL can be employed to clean it up.

This hard macro features an adjustable-bandwidth capability. It lets users simply dial in the amount of desired-period jitter filtering. The bandwidth-filter amount is designed to adjust as a precise fraction of the reference frequency. To be exact, it goes from 1 to 500th of the reference frequency.

Other characteristics of the Low-Bandwidth PLL include a power dissipation of 5 mA at around 400 MHz (/1 output) in TSMC 0.13-μm LV process technology. This PLL's maximum area is approximately 0.20 mm^2 including isolation. Its supply voltage is 1.0 V +/–10% and it operates with junction temperatures from –40° to 125°C.

The Spread-Spectrum PLL, on the other hand, is designed to generate a sawtooth-frequency-output waveform with an adjustable spreading rate between 15 KHz and 4 MHz. Given the reduced bandwidth, the feedback divider includes 8 fractional bits to allow the frequency to be set more precisely. Compared to the Low-Bandwidth PLL, the bandwidth is adjustable over a lower range. This feature enables it to work well with the spreading function. The spreading amount is typically adjusted in the range of 0% to 1%. The actual range, however, is much wider. It also is a function of the spreading rate.

Other specific characteristics of the Spread-Spectrum PLL include a nominal power dissipation of 5 mA at around 400 MHz (/1 output) in TSMC 0.13-μm LV process technology. The PLL's maximum area is roughly 0.20 mm^2 including isolation. Its supply voltage is 1.0 V +/–10%. This PLL operates with junction temperatures from –40° to 125°C.



2. This plot depicts clock spectrum. The amplitude in dB is plotted as a function of frequency. Because of the broadened frequency spectrum, peaks in the EMI emission spectrum from the electronic devices using spread-spectrum clocks are similarly lower with corresponding flattened peaks.

Both the Spread-Spectrum and Low-Bandwidth PLLs support most standard CMOS processes from foundries like TSMC and UMC. True Circuits can accommodate specific customer requests for porting to other process technology. Consider the Low-Bandwidth PLL in TSMC 0.13-μm LV process technology. It has an adjustable bandwidth of Fref/(10χx), where x varies from 1 (the maximum bandwidth possible for any PLL) to 512. The feedback divider includes 8 fractional bits. The period jitter is specified at a maximum of +/–2.5% under worst-case noise conditions.

The low-jitter Spread-Spectrum PLL and Low-Bandwidth PLL are both sampling. They are available for a per-use license fee with no royalty fees. Included in the licensing fee is integration support to ensure a successful tape out. The deliverables include GDSII and LVS Spice netlist, behavioral, synthesis, and Library Exchange Format (LEF) models, as well as extensive user documentation. ■

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