24.2: Self-Biased, High-Bandwidth, Low-Jitter 1-to-4096 Multiplier Clock Generator PLL

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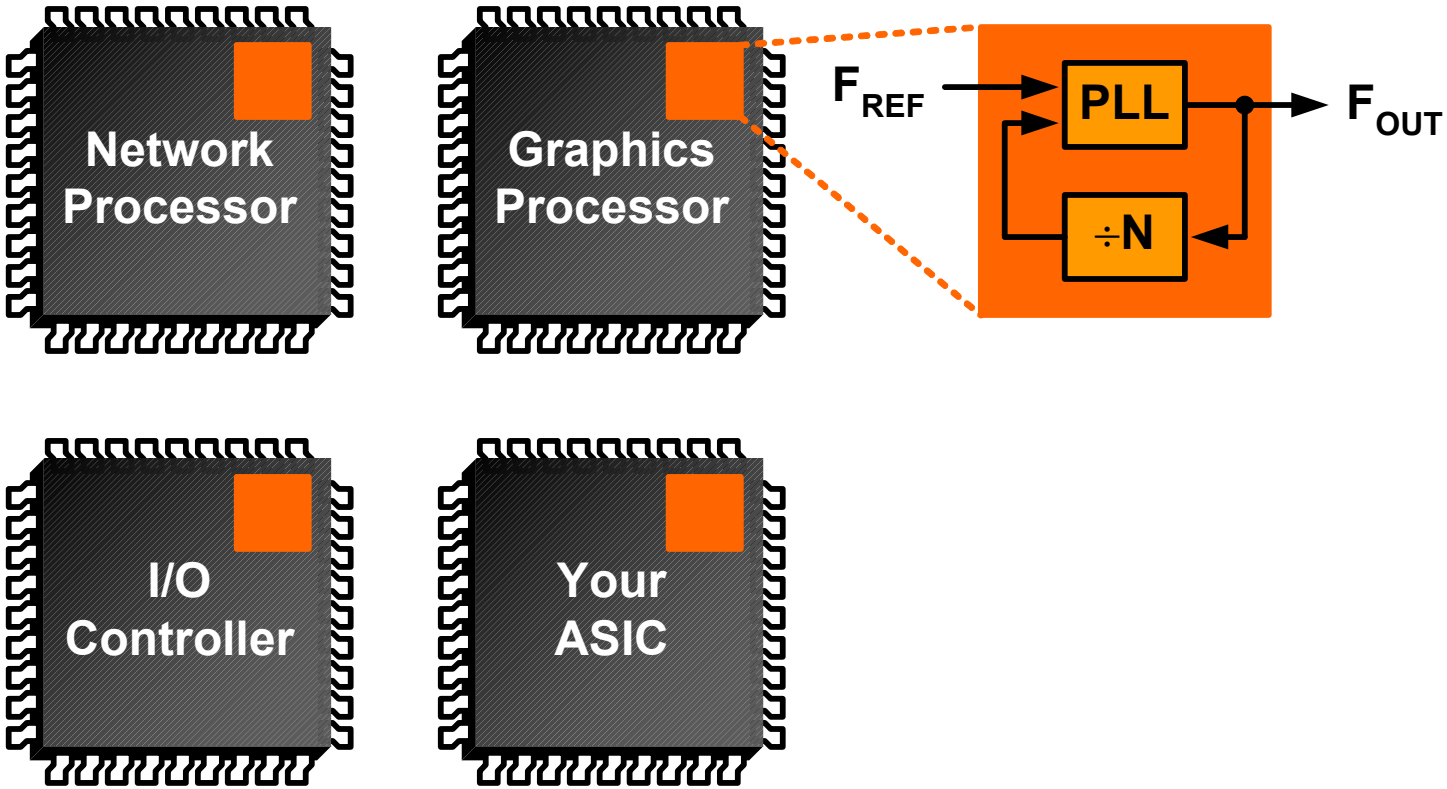
Clock Generator PLLs for ASICs



- Most ASICs PLLs for clock generation, but …
  - Use different frequencies and multiplication

Optimal PLL Design

- For each F_{OUT} and N, one must adjust loop parameters for both minimum jitter and stability

- For clock generators (track input clocks)
  ($\omega_{REF} = 2\pi \cdot F_{OUT}/N$)
  - Loop bandwidth : $\omega_N \sim \omega_{REF}/20$
  - Damping factor : $\zeta \sim 1$
  - Third-order pole : $\omega_C \sim \omega_{REF}/2$

- Circuit parameters (e.g. I_{CH}, R) must vary with F_{OUT} and N!

Addressing Diverse Specifications

- Designing a different PLL for each ASIC
  - Easier to meet the specification, but …
  - Verifying all designs is difficult and costly

- Our Goal: One PLL design for all ASICs
  - Only one design needs verification, but …
  - Loop parameters must adjust automatically to satisfy wide range of F_{OUT} and N

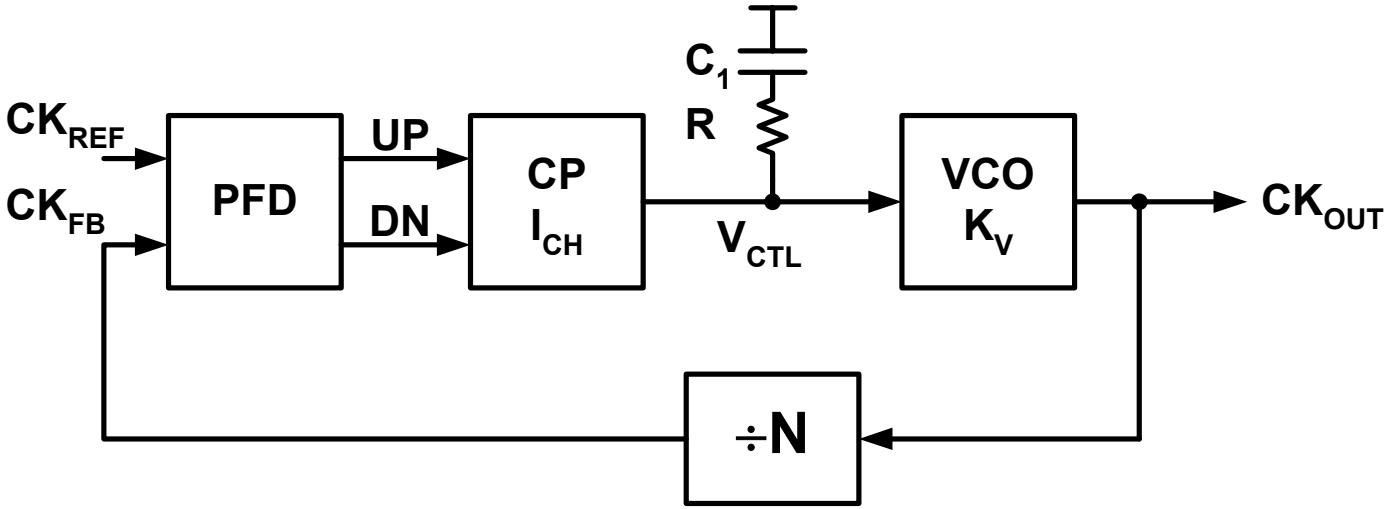
Challenges

- Self-biased PLLs [Maneatis '96] adjust for F_{OUT}
  - Achieve fixed ω_N/ω_{REF} and ζ indep. of PVT
- But, Self-Biased PLLs do NOT adjust for N
  - ω_N/ω_{REF} and ζ vary with N (want fixed)
  - ω_C/ω_{REF} varies with N (want fixed)
- This talk extends Self-Biased PLLs for wide ranges of N with a new loop filter network

Outline

- Introduction
- Review of Self-Biased PLLs
- Pattern Jitter Issues
- Loop Filter Architecture
- Implementation of Key Circuits
- Measured Results
- Conclusions

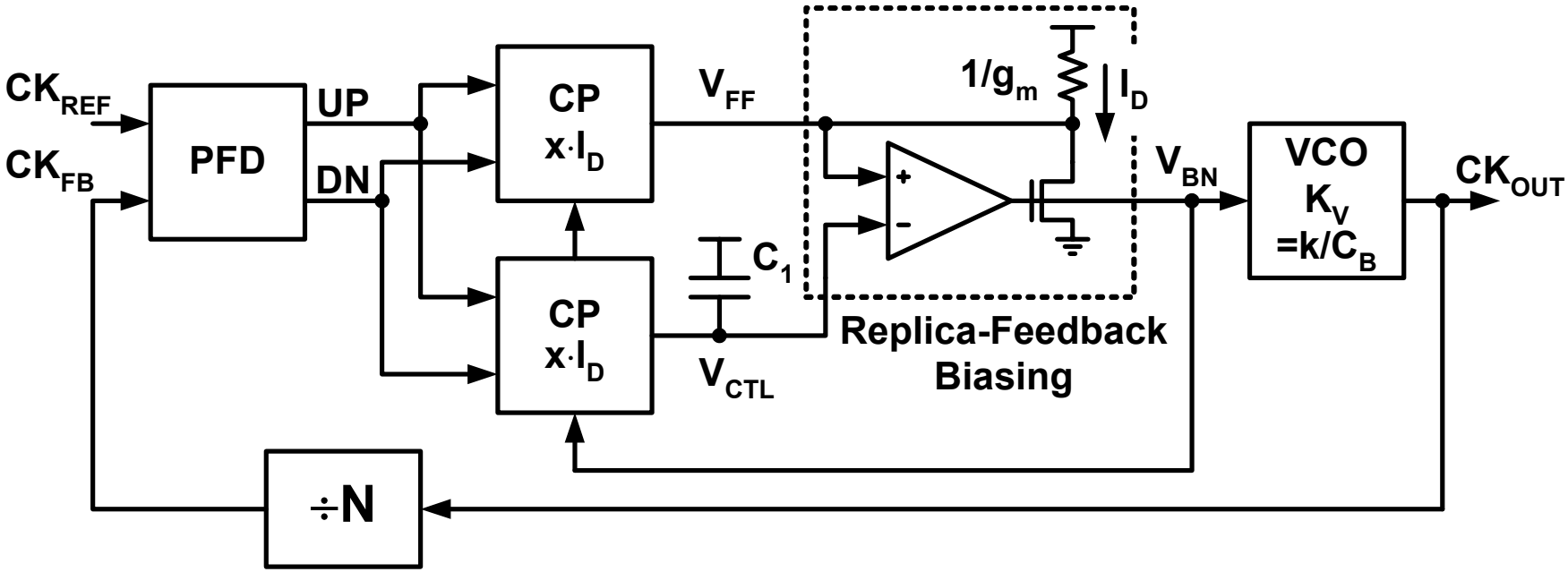
Second-Order PLLs



$$\frac{P_O(s)}{P_I(s)} = N \cdot \frac{1 + 2 \cdot \zeta \cdot (s/\omega_N)}{1 + 2 \cdot \zeta \cdot (s/\omega_N) + (s/\omega_N)^2}$$

$$\omega_N = \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_V \cdot \frac{1}{C_1}} \qquad \zeta = \frac{1}{2} \cdot \omega_N \cdot R \cdot C_1$$

Self-Biased PLLs



$$R = 1/g_m \qquad I_{CH} = x \cdot I_D \qquad F_{VCO} = g_m/C_B$$

Self-Biased PLLs

- With Self-Biased PLLs

$$\omega_N/\omega_{REF} = \frac{1}{2\pi}\cdot\sqrt{x\cdot N}\cdot\sqrt{C_B/C_1} \sim \sqrt{x\cdot N}$$

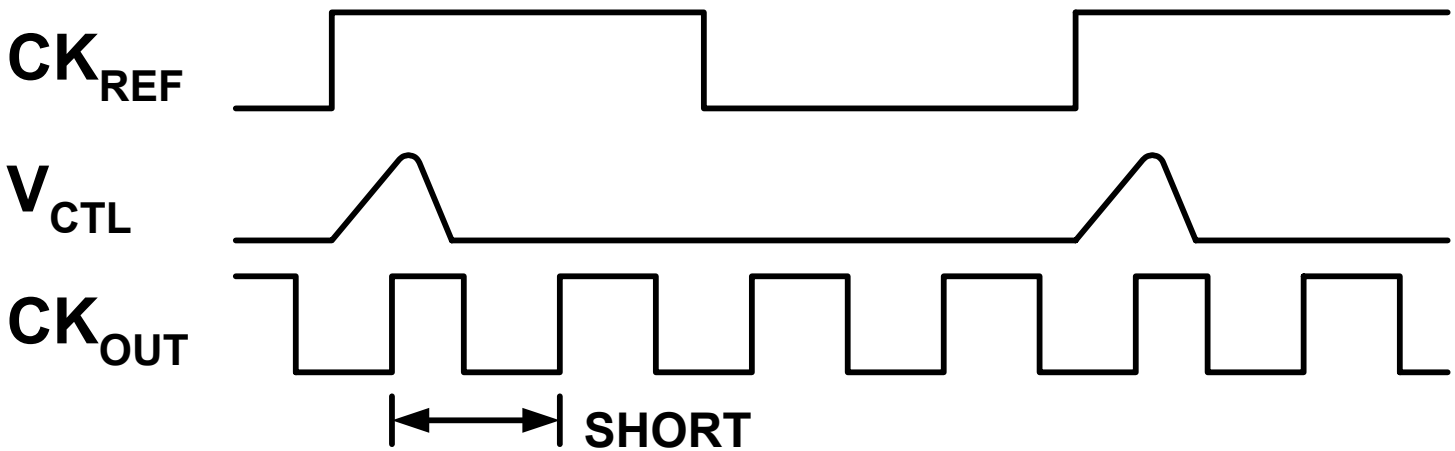
$$\zeta = \frac{1}{4}\cdot\sqrt{x/N}\cdot\sqrt{C_1/C_B} \sim \sqrt{x/N}$$

  - ω_N/ω_{REF} and ζ are constant with F_{OUT},

    BUT not with N

Pattern Jitter / Spurious Noise

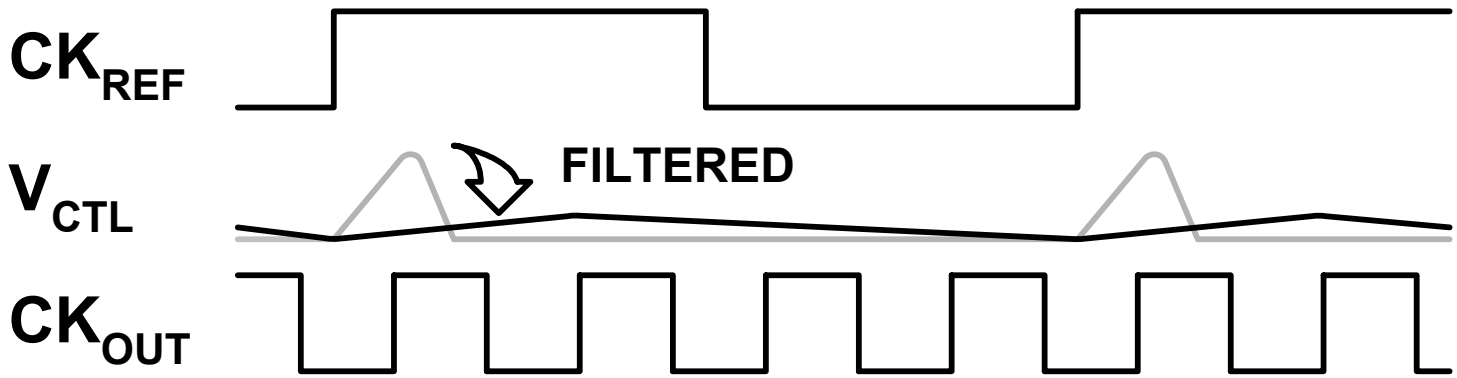
- Phase corrections every rising reference edge can cause disruptions to nearby output cycles
  - Periodic noise pattern repeats every ref. cycle or N output cycles



- Typical causes
  - Charge pump imbalances or leakage
  - Jitter in reference clock (aperiodic result)

Shunt Capacitor

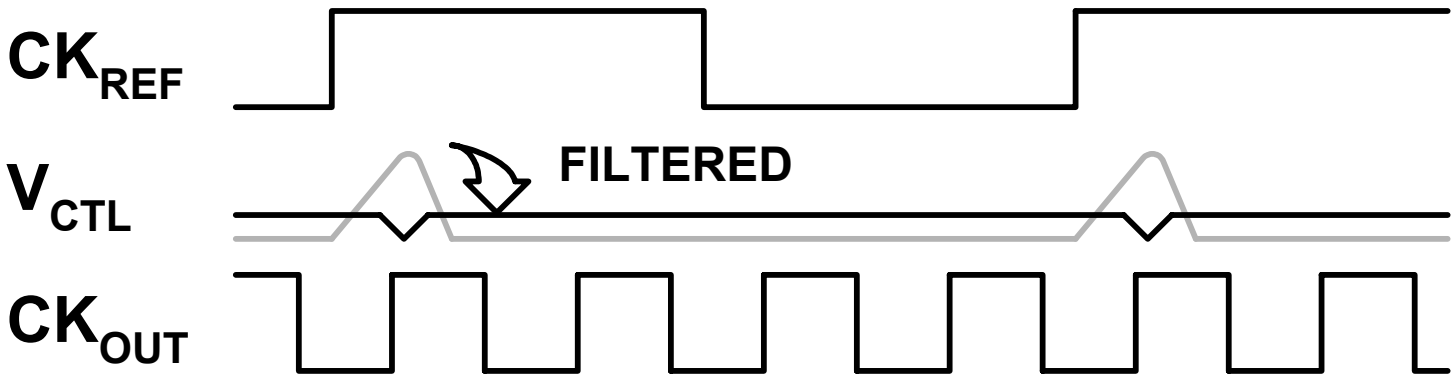
- Use third-order pole to extend disturbance with reduced amplitude over many output cycles



- Problem with varying N using fixed capacitor
  - Extended number of cycles NOT function of N
  - Too few for large N → Pattern jitter
  - Too many for small N → Instability

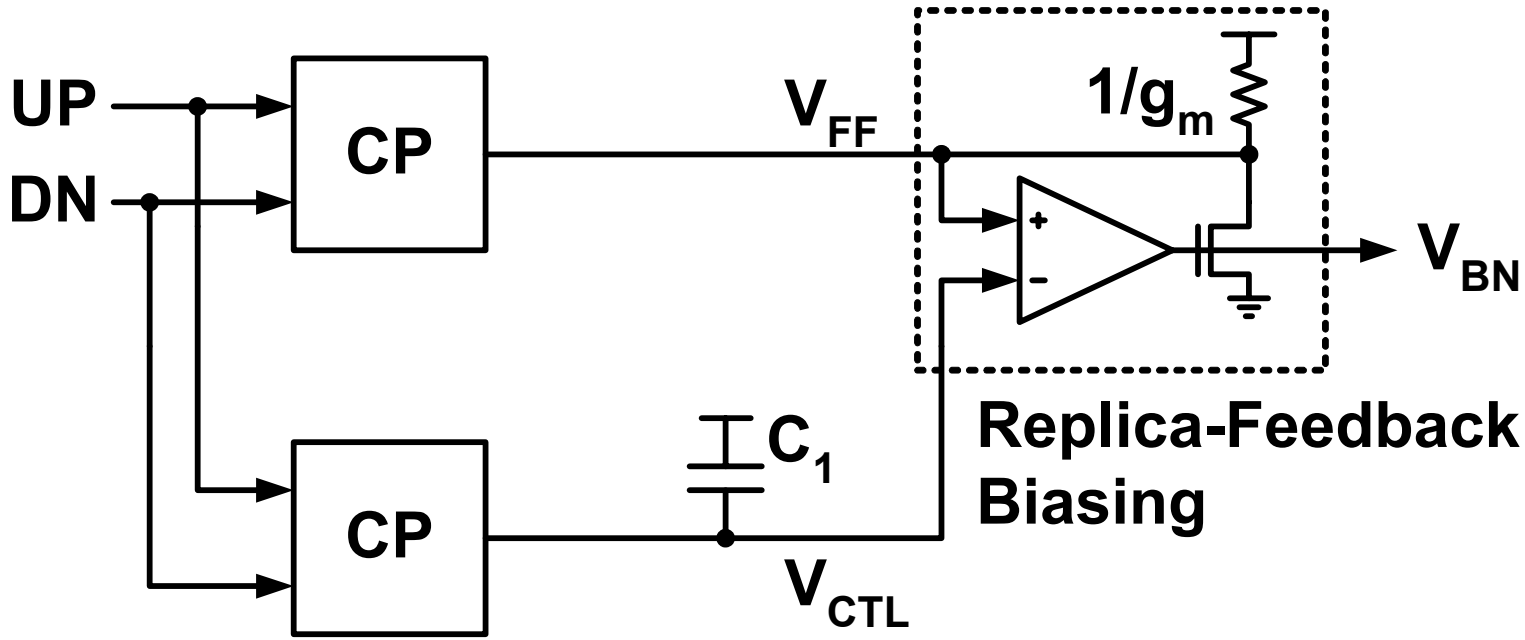
Proposed Loop Filter

- Use switched capacitor filter network to
  - Output scaled amplitude error signal with N output cycle duration [Maxim ’01]



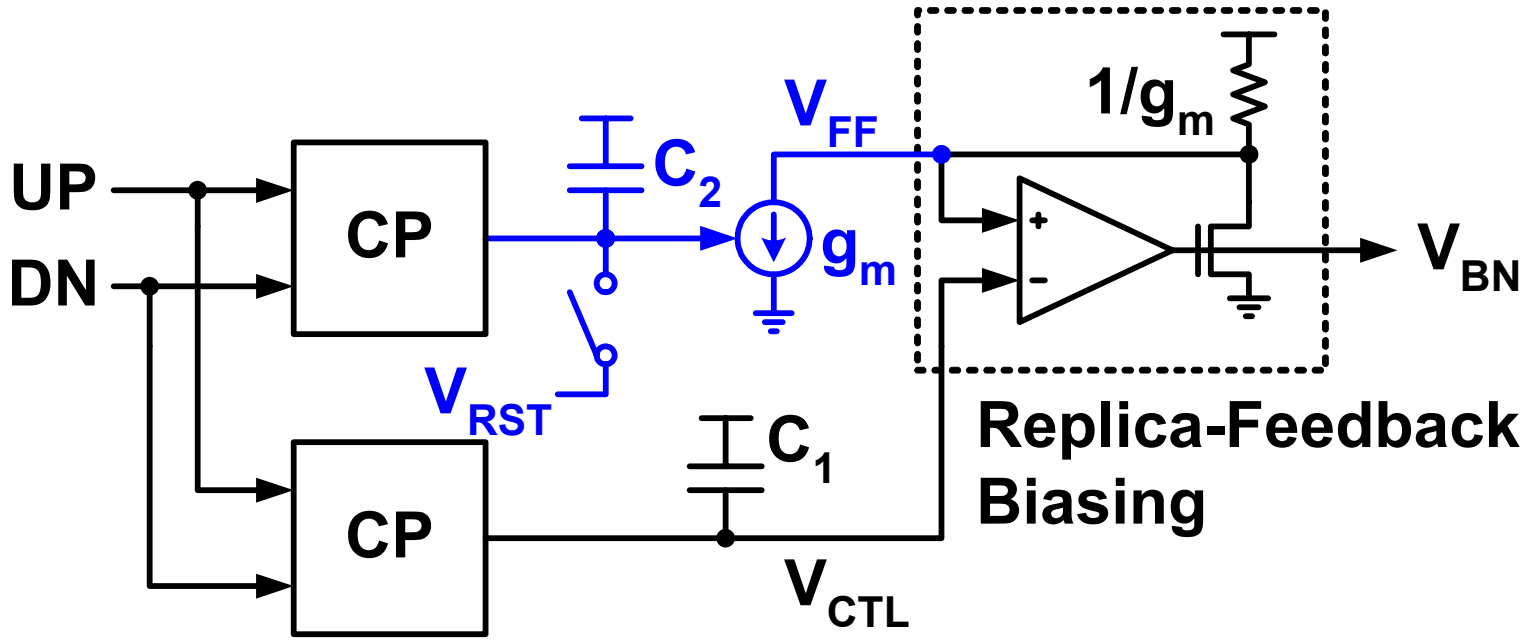
- Want a simple solution using this approach that is compatible with Self-Biased PLLs

Original Filter Network



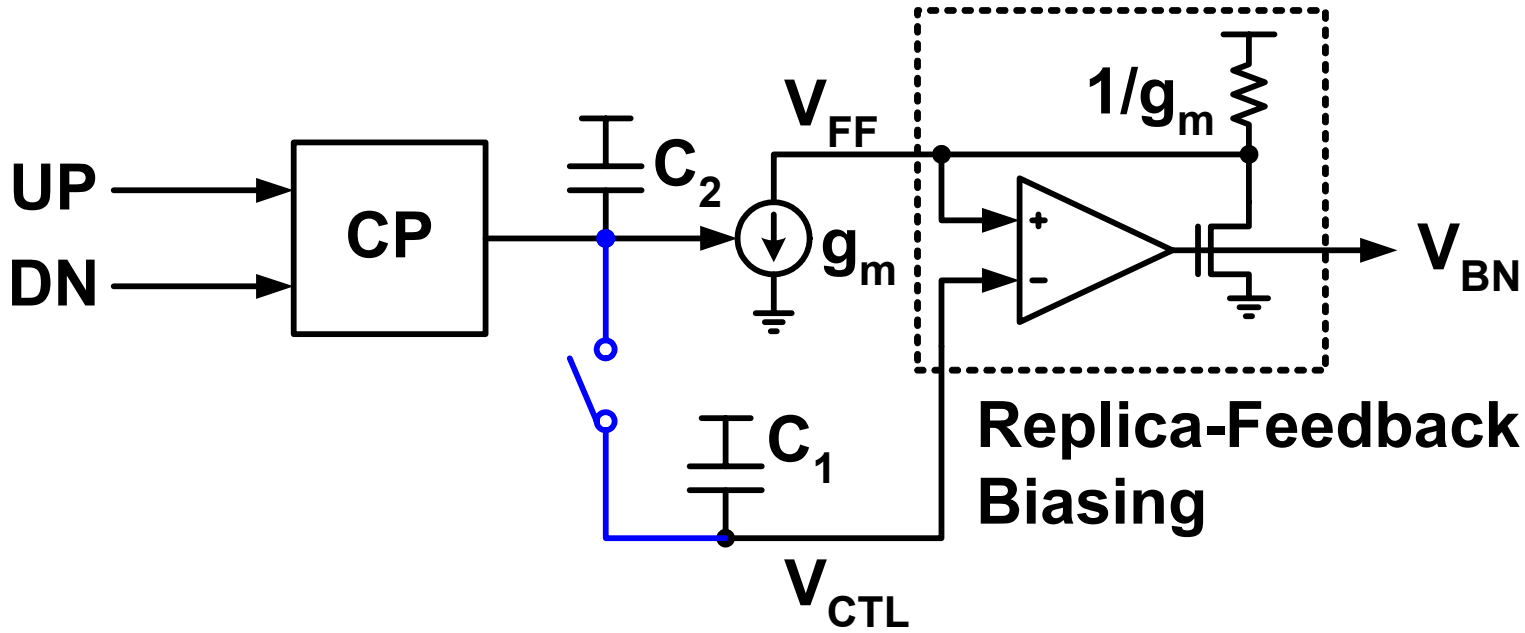
- Only need to filter feed-forward path

Sampled Feed-Forward Network



- Sample phase error and generate proportional current that is held constant for $N \cdot T_{OUT}$
- Sampled error is reset at end of ref. cycle
  - Need $V_{RST} = V_{CTL}$ as zero bias level

Complete Filter Network



- Reset C_2 to V_{CTL} directly
  - Eliminates C_1 charge pump
- Equivalent feed-forward control gain

  $Q_O \sim N \cdot Q_I$

Loop Dynamics

- With this new loop filter network we achieve

$$\omega_N/\omega_{REF} \sim \sqrt{x \cdot N} \qquad \zeta \sim (Q_O/Q_I) \cdot \sqrt{x/N} \sim \sqrt{x \cdot N}$$

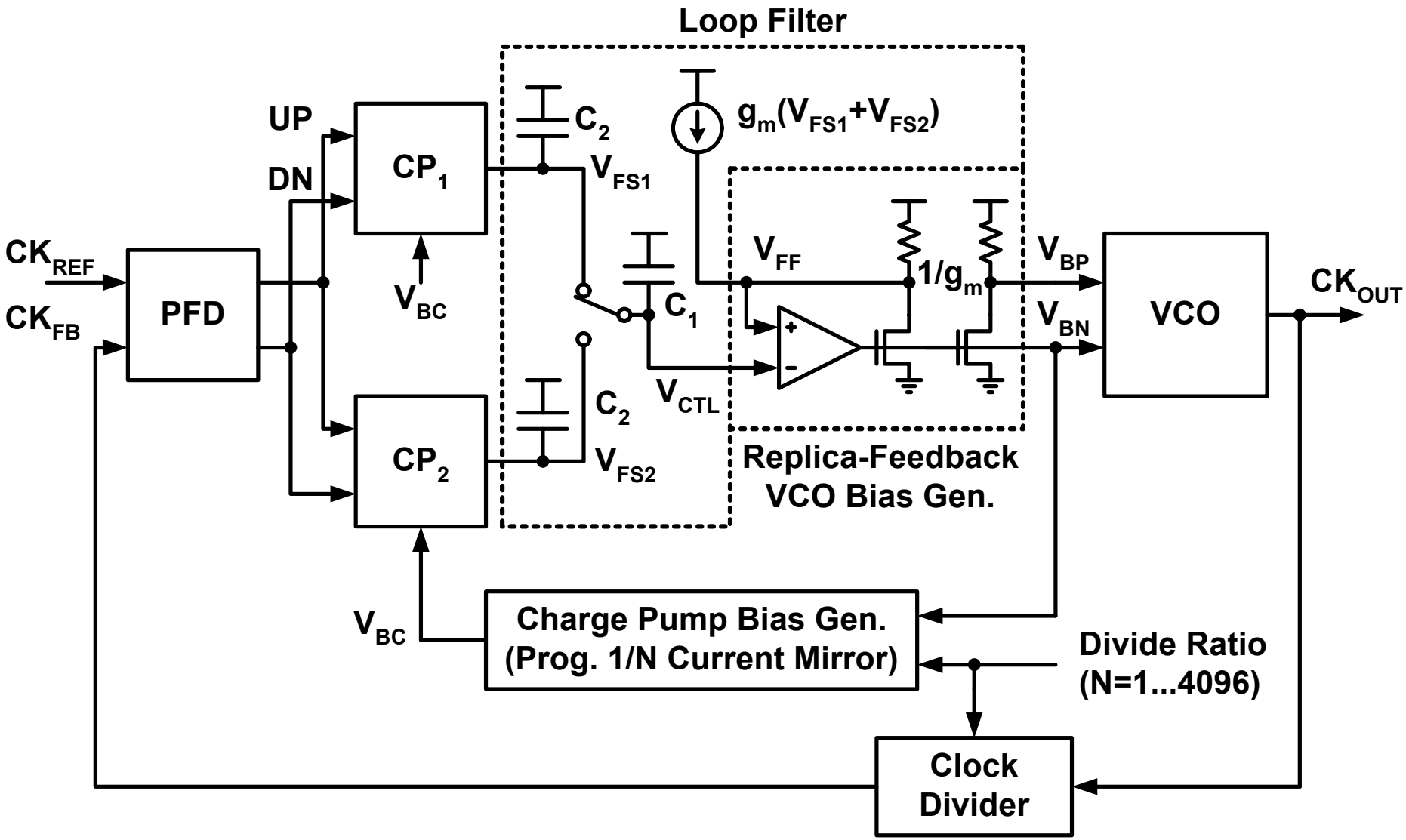
- Need to keep ω_N/ω_{REF} and ζ constant with N
  - Just scale charge pump current with 1/N (=x)
- More detailed analysis will show

$$\omega_N/\omega_{REF} = \frac{1}{2\pi} \cdot \sqrt{C_B/C_1}$$

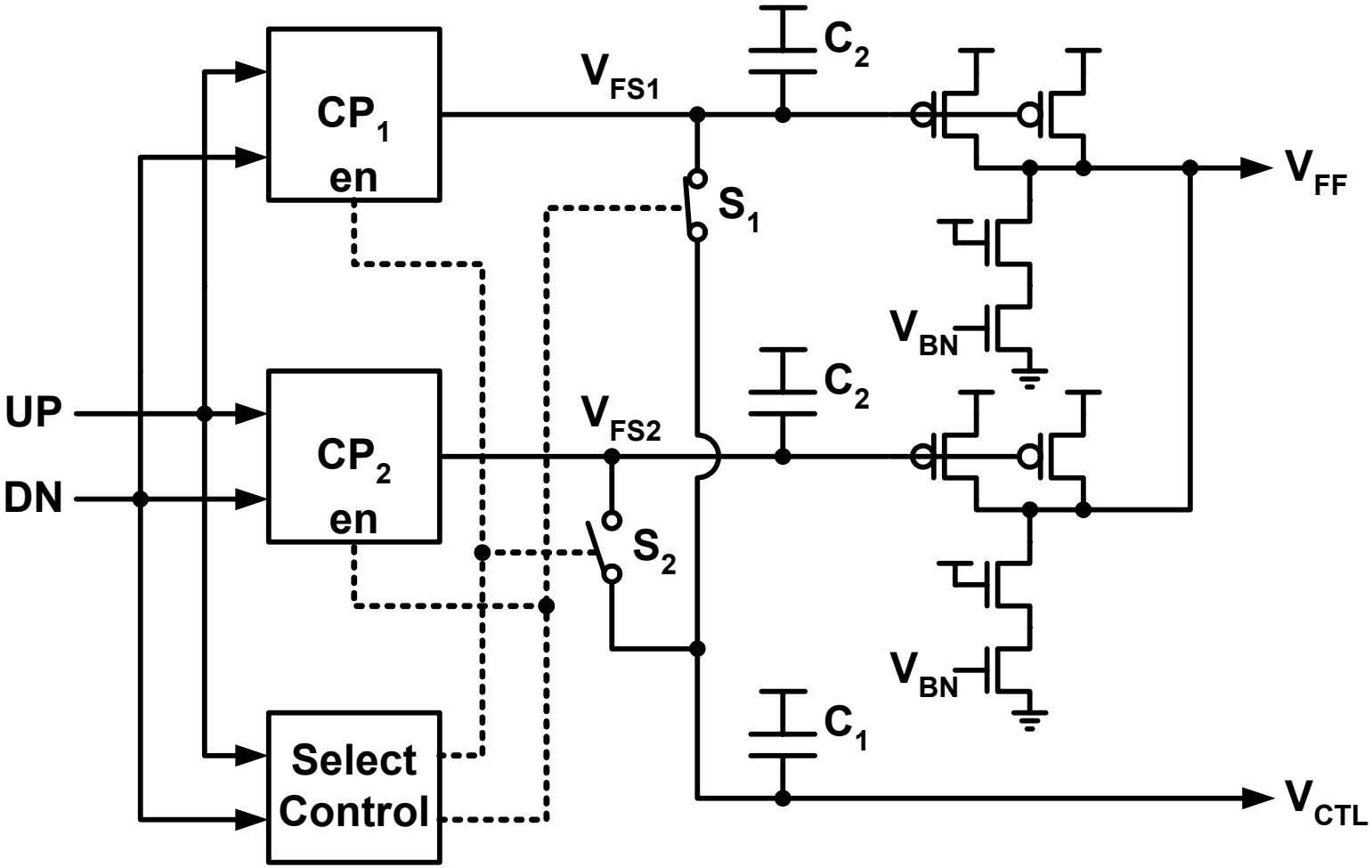
$$\zeta = \frac{1}{4} \cdot \sqrt{C_B \cdot C_1}/C_2$$

  - Both are independent of F_{OUT}, N, and PVT!

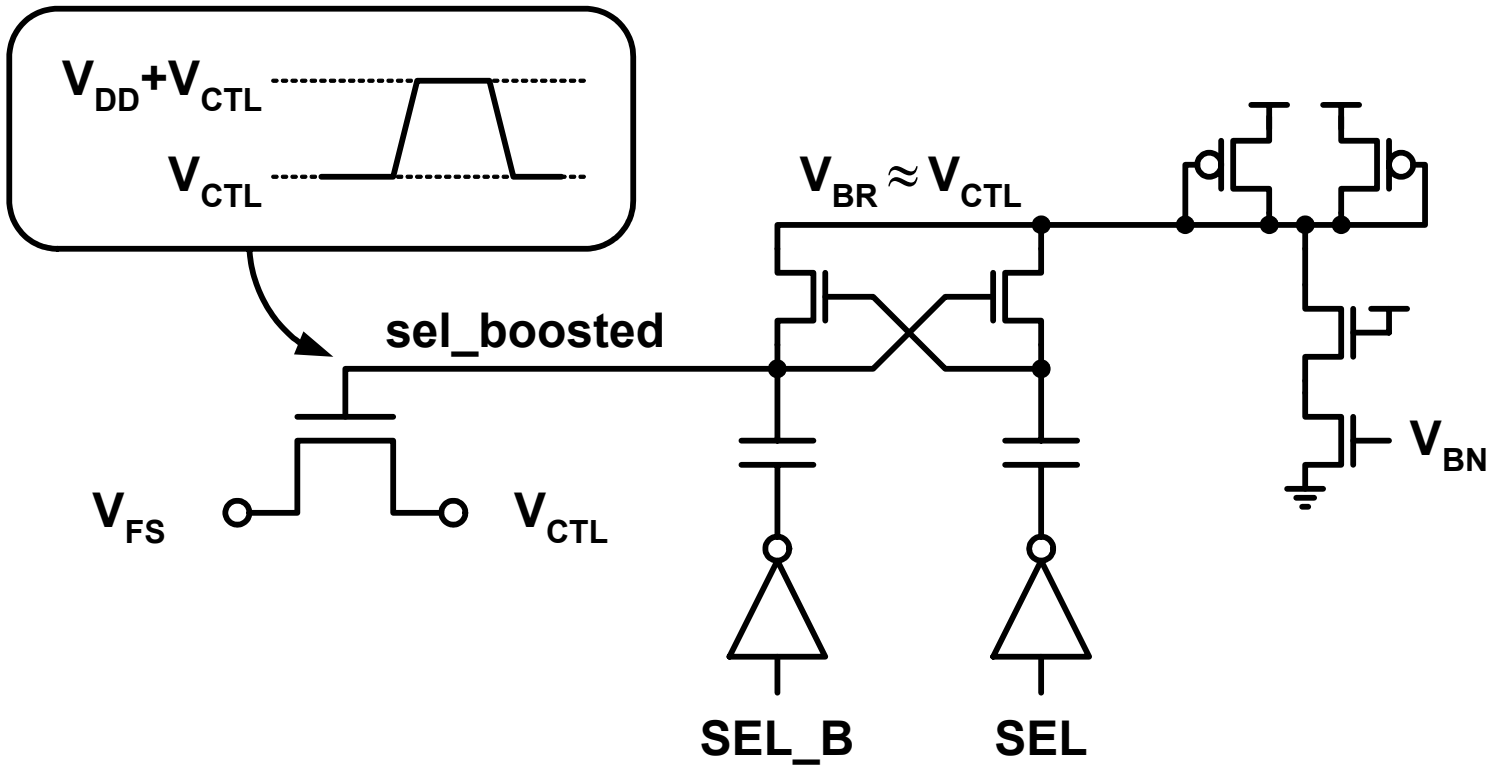
Complete Self-Biased CGPLL



Self-Biased Filter Network



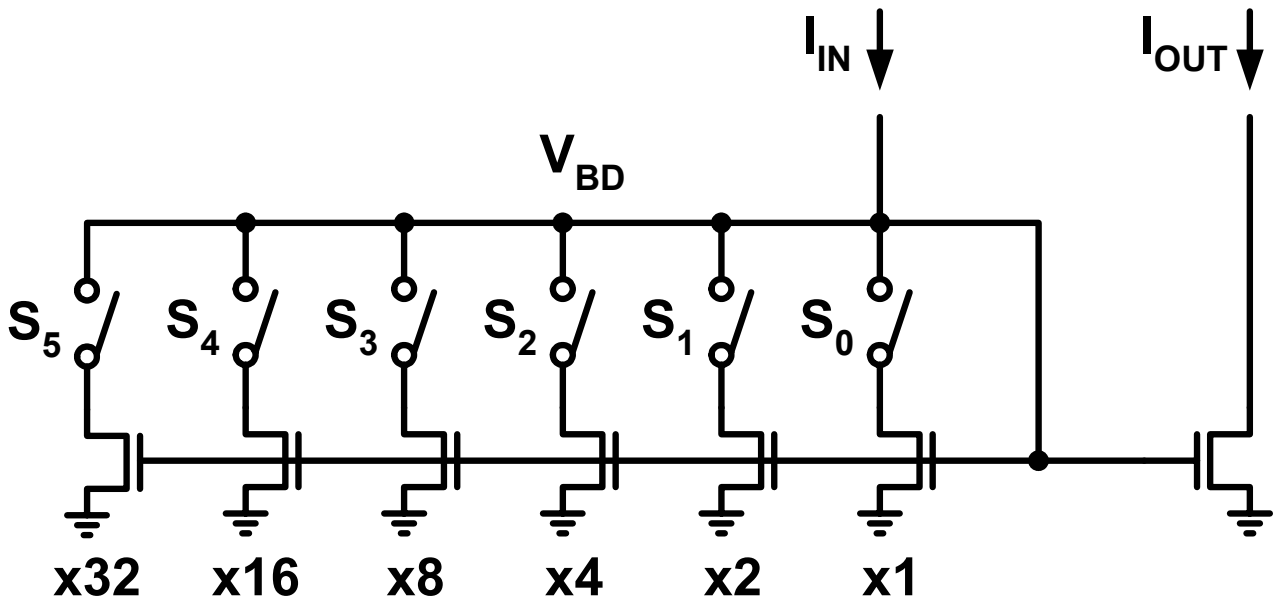
Filter Network Reset Switches



- Can switch to V_{CTL} independent of voltage level

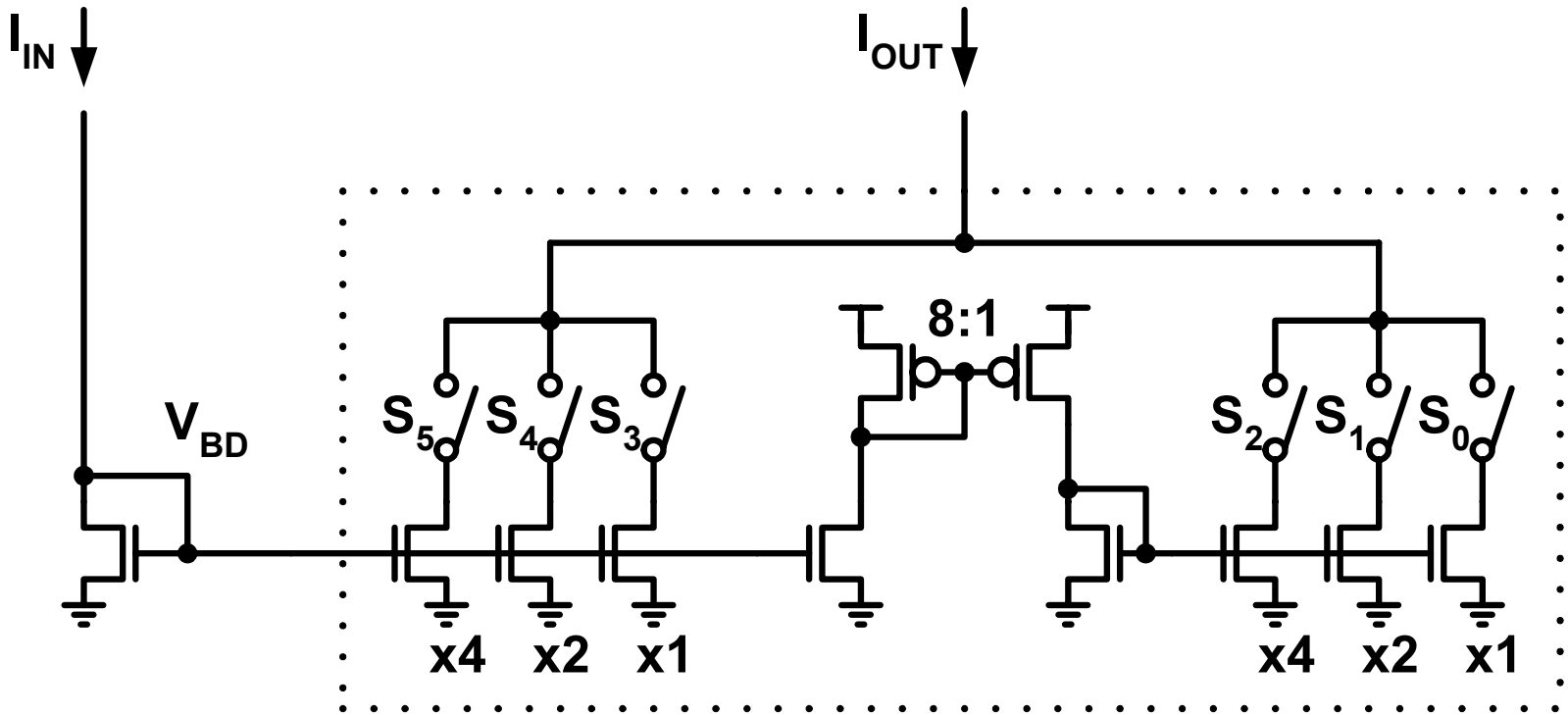
Inverse-Linear Current Mirror

- Need to generate $I_{CH} = I_D / N$
- Use switches to adjust device size on input side
  - For N=1~4096, need 12 binary weighted legs
  - Need size range of 2048:1 → Too much area!



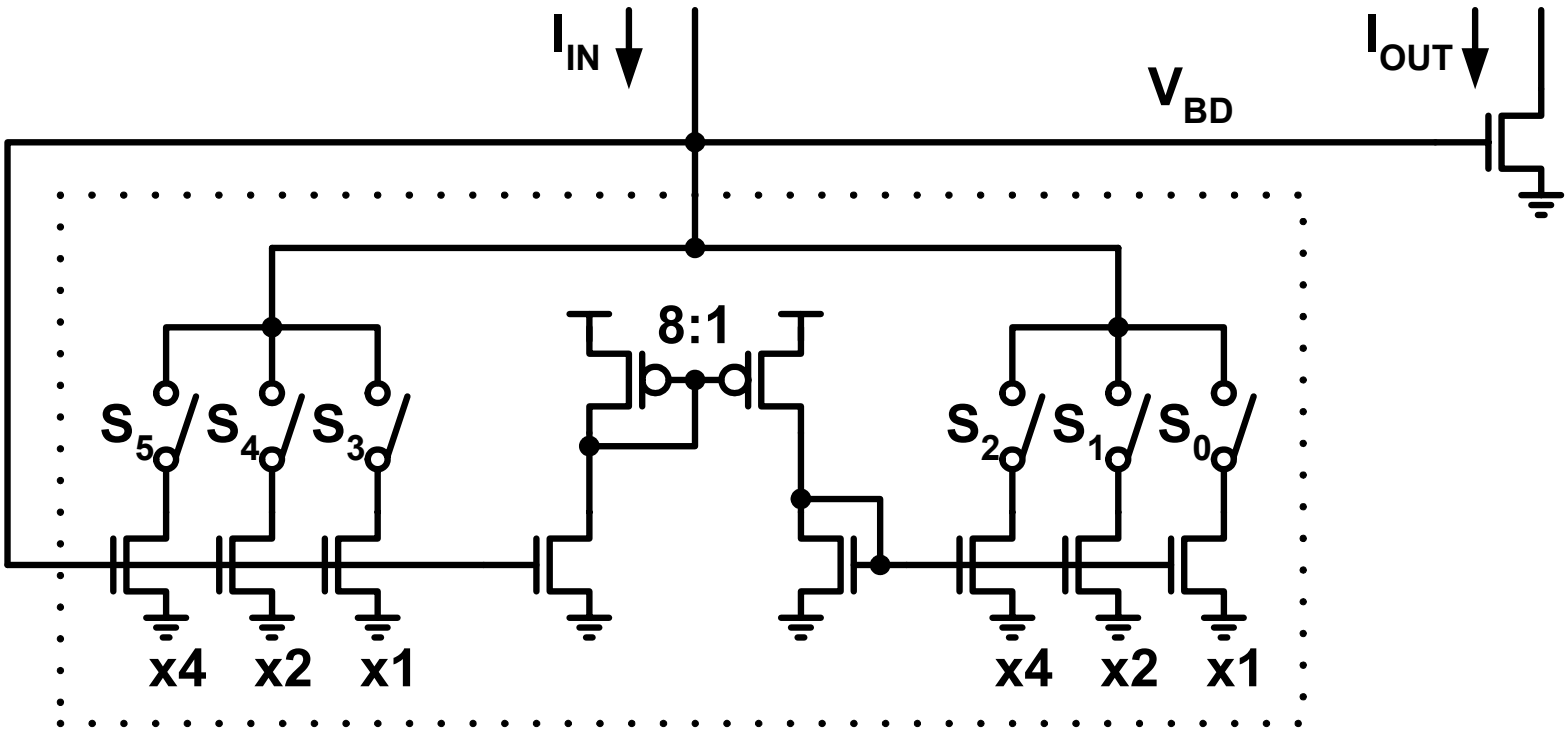
Multi-Stage Linear CM

- Solution to size problem with LINEAR control
  - Use multiple device groups operating at different but ratioed current densities
  - Can have large ranges using small devices

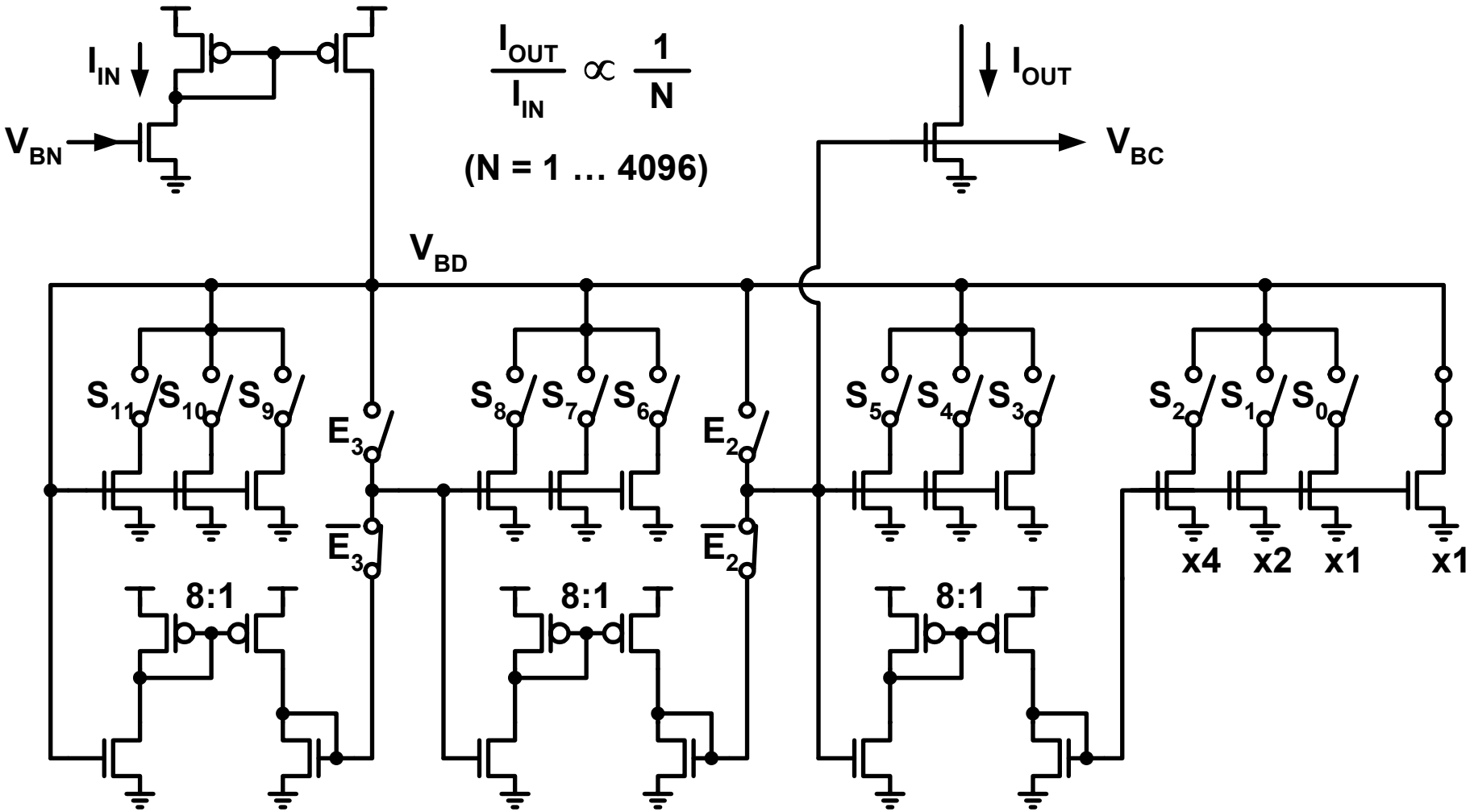


Multi-Stage Inverse-Linear CM

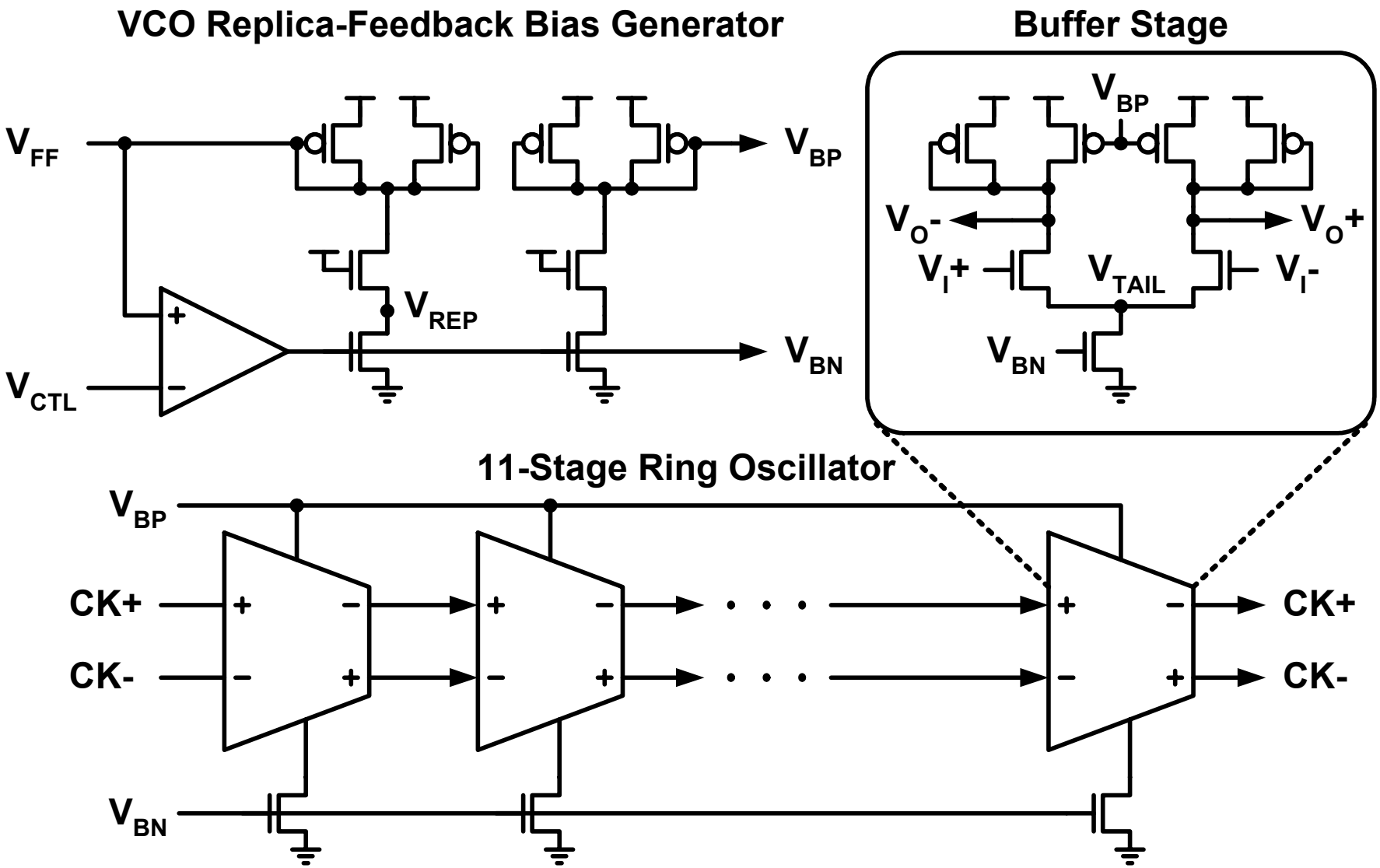
- Just diode connect multi-stage linear current source and use as input side of current mirror
  - Can output gate bias of any device group
  - Stable as long as gain blocks reduce currents



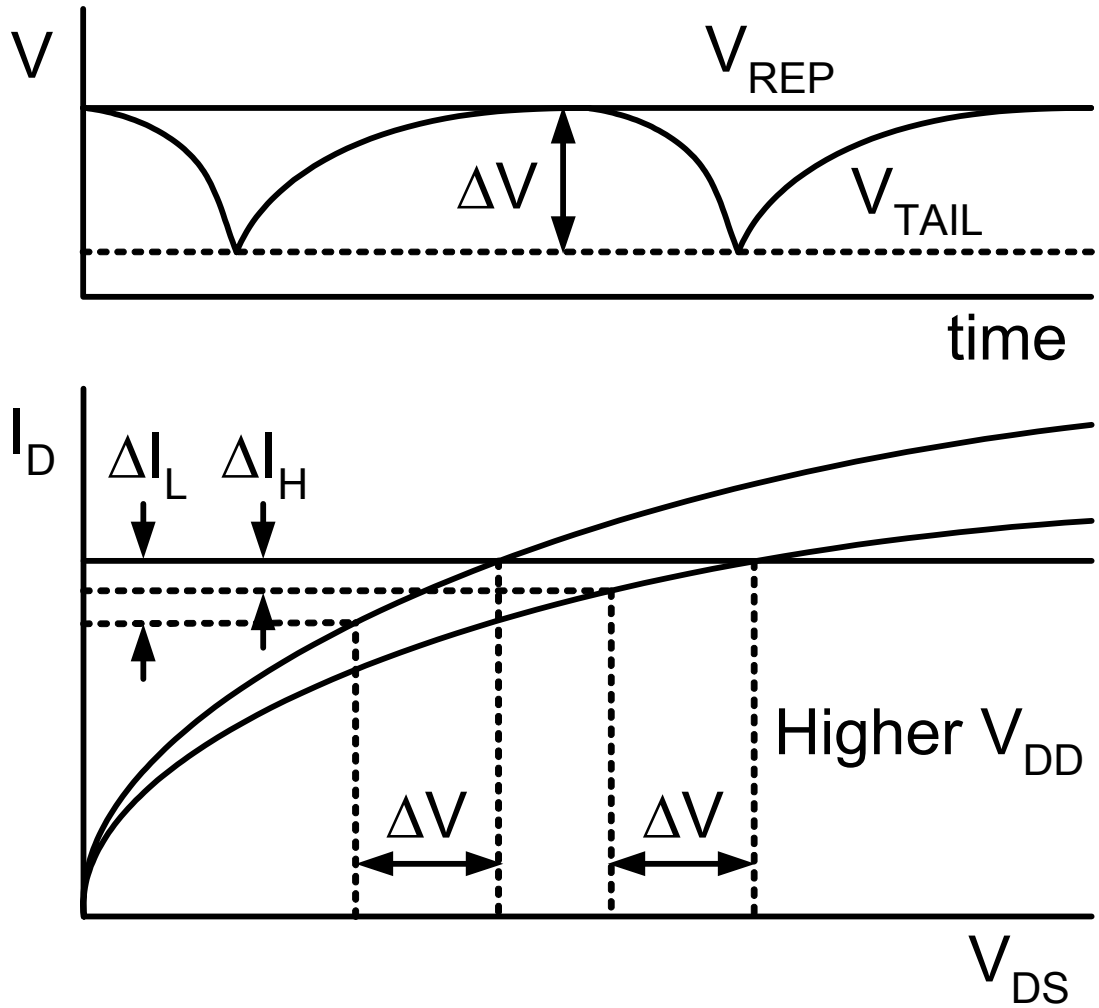
Complete Current Mirror



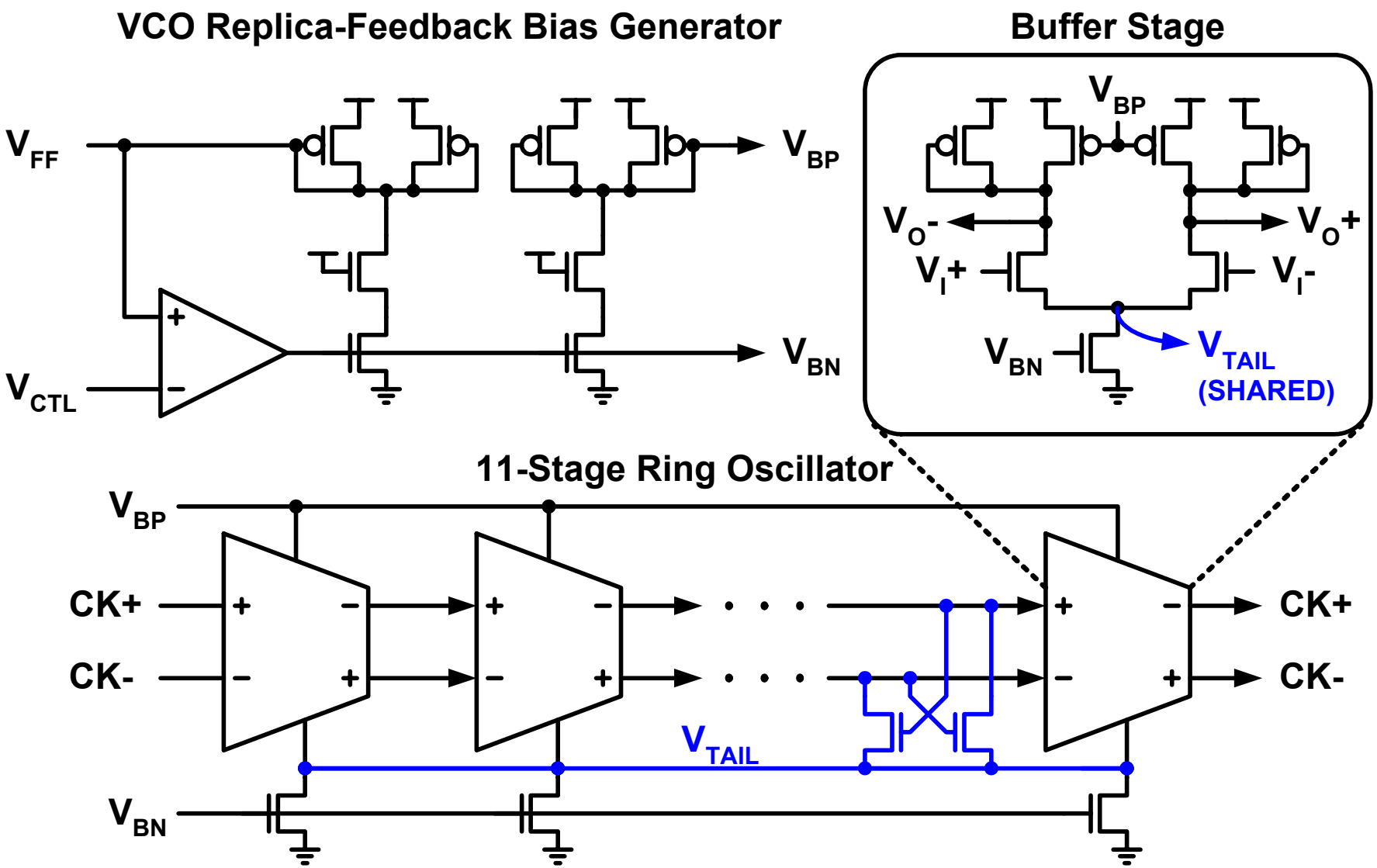
Voltage-Controlled Oscillator



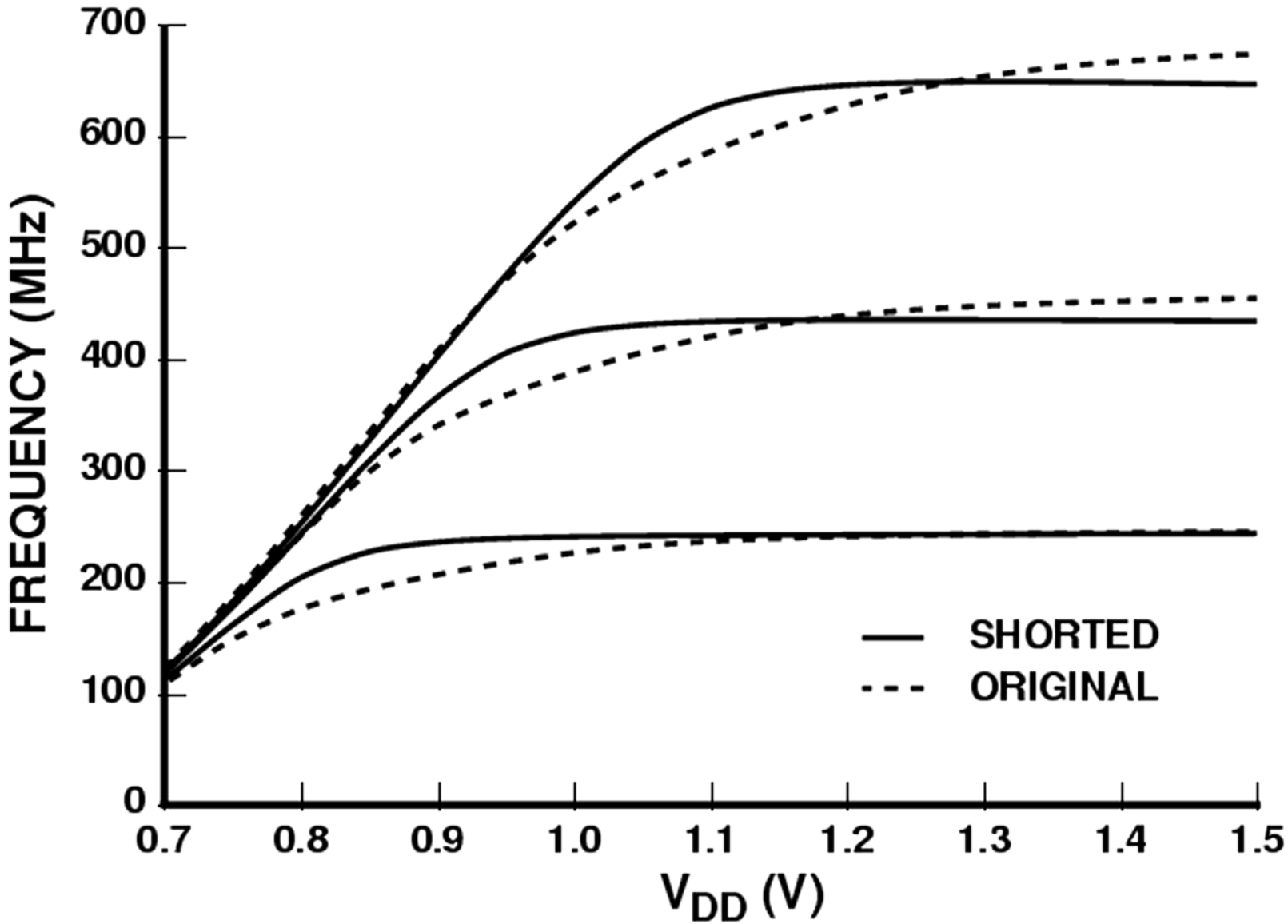
Buffer Tail Node Matching



Modified VCO

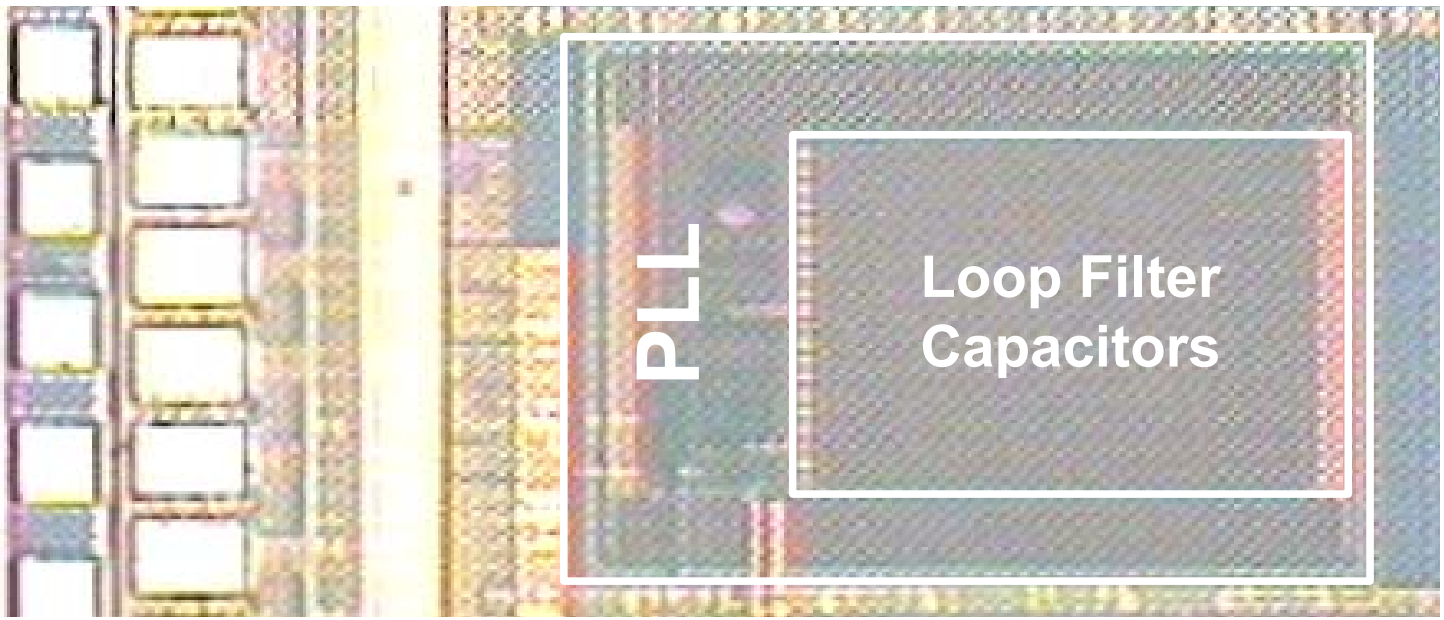


Static Supply Sensitivity

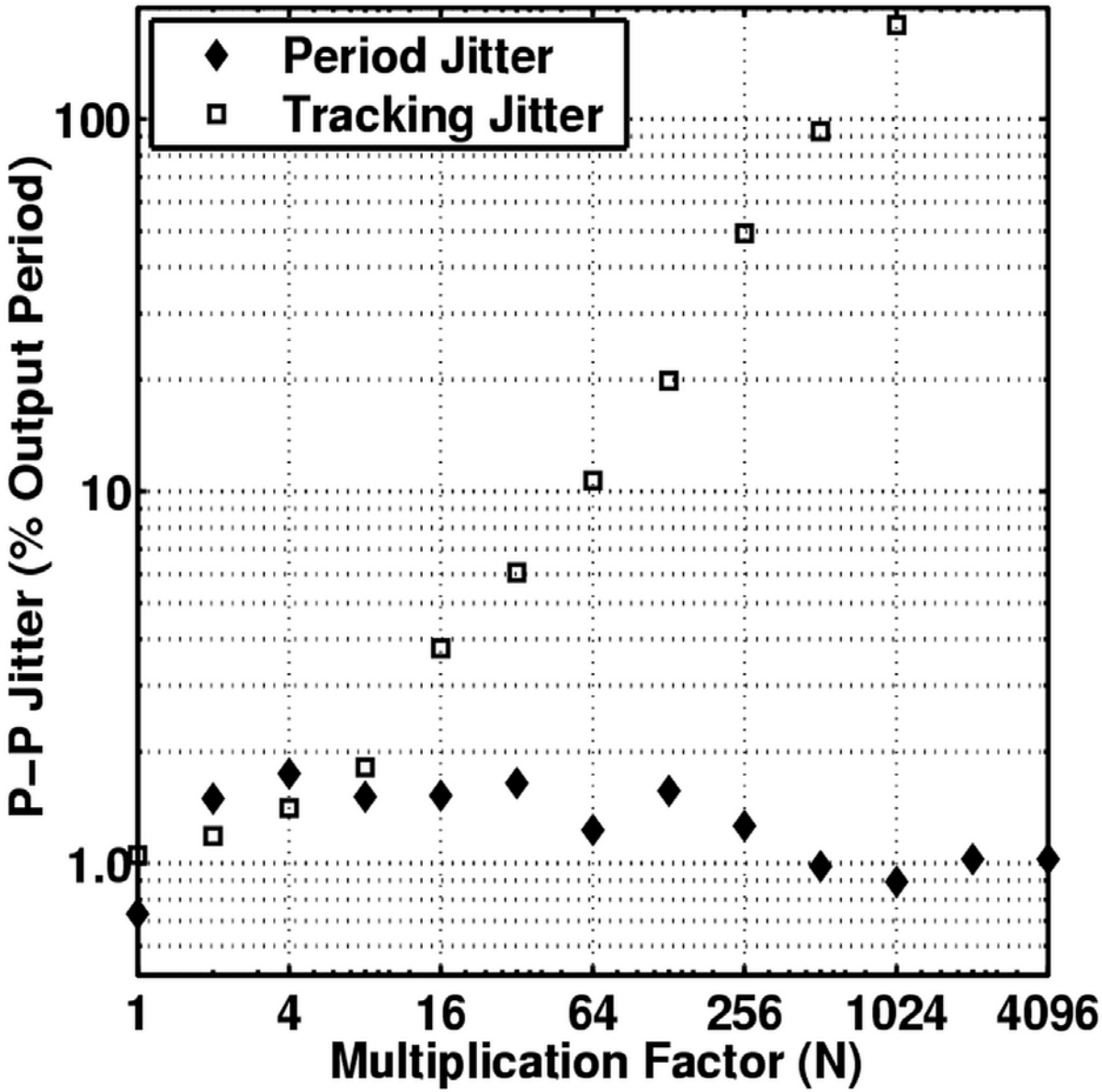


PLL Implementation

Process Technology	0.13μm N-well CMOS
Nominal Supply Voltage	1.5V (designed for 1.2V)
Total Occupied Area	0.38 x 0.48mm^2
VCO Frequency Range	30 ~ 650 MHz
Multiplication Factor Range	N = 1 ~ 4096
Power Dissipation	7mW @ 240 MHz, 1.5V



Measured Jitter vs N (240MHz)



Conclusions

- Proposed PLL achieves wide N and F_{OUT} range
- PLL is self-biased with constant loop dynamics (ω_N/ω_{REF}, ζ), independent of N, F_{OUT} , and PVT
- Sampled feed-forward network suppresses pattern jitter with effective ω_C that tracks ω_{REF}
- Achieves relatively constant period jitter of less than 1.7% as N is scaled from 1 to 4096