TA 7.5: Precise Delay Generation Using Coupled Oscillators*

John G. Maneatis, Mark A. Horowitz

Stanford University, Stanford, CA

Precise delay generation is a necessity in state-of-the-art integrated test and measurement chips[1]. High time resolution is difficult to achieve. It requires precise delays significantly smaller than an intrinsic gate delay. Precise delays with gate-delay resolution can be achieved by phase locking a ring oscillator to an established clock. An array oscillator, a series of coupled ring oscillators, achieves a delay resolution equal to a buffer delay divided by the number of rings. Using a 2μm n-well CMOS technology, delays as small as 30ps are achieved at frequencies up to 200MHz.

An array oscillator structured as a two-dimensional array of buffers is shown in Figure 1. The rings extend horizontally and are coupled vertically. Coupling between rings is by an additional input on each buffer of each ring. The transition time of the coupling input with respect to the ring input affects the output delay of each buffer. Lagging coupling inputs increase delay, while leading coupling inputs decrease delay. With the array closed in a loop around the top and bottom, the high degree of symmetry makes an individual buffer and its interconnections to neighboring buffers indistinguishable from all other buffers in the array. From this symmetry, all nodes in the array oscillate at the same frequency in steady state and the output delays of all buffers in the array are equal. Furthermore, the phase differences between the coupling input and ring input of all buffers in the array are equal since they determine the output delays of the buffers. Thus, all the rings oscillate at the same frequency while maintaining a precise phase relationship to one another.

If the series of rings is left open or if it is closed into a loop so top array nodes T_i connect to corresponding bottom array nodes B_i the phase difference between ring nodes in a given buffer position will be zero. However, if the series of rings is closed so nodes T_i connect to nodes B_{i-2}, the phase difference across all corresponding ring nodes will uniformly span, from top to bottom of the array, negative two buffer delays in phase. Thus, the difference in phase between adjacent rings is two buffer delays divided by the number of rings. Because the boundary conditions are periodic with 2π radians of phase, corresponding to 2N buffer delays, other mutually-exclusive modes of oscillation are possible, the number being in part limited by the bandwidth of the buffer stages. Each mode will oscillate at a different frequency.

An array oscillator with 17 rings each with 5 buffers with nodes T_i connected to nodes B_{i-2} gives rise to three possible modes of oscillation of progressively lower frequency, where the phase difference across all corresponding ring nodes is -2, -12, or -22 buffer delays. The array is selectively reset in a particular mode by initializing the phase relationship among the nodes of the array so that it is close to that of the desired mode by switching of the ring bias lines.

The buffer stage is based on an nMOS source-coupled pair with symmetric load elements and a dynamically-biased simple nMOS current source as shown in Figure 2. The coupling input is formed from an additional source-coupled pair sharing the same loads and current source. The symmetric loads are non-linear elements that have I-V characteristics symmetric about the center of the voltage swing. A symmetric load is readily realized as a diode-connected pMOS device in shunt with an equal-size biased pMOS device. With the top supply as the upper swing limit, the lower swing limit is symmetrically opposite at the bias level for the biased pMOS device (V_{CTRL}). Thus, buffer output swings vary with V_{CTRL} rather than being fixed in order to maintain the symmetric I-V characteristics of the loads as shown in Figure 3.

Symmetric loads, although non-linear, provide for high dynamic supply-noise rejection. Non-linear load resistances typically convert common-mode noise into differential-mode noise affecting buffer delays. With symmetric loads, however, the first-order non-linear noise coupling terms cancel out, leaving only the higher-order terms, substantially reducing jitter caused by common-mode noise. SPICE simulations of the array with worst-case coupling of buffer output interconnection capacitance show that a 500mV supply-voltage bump results in total phase error of 0.5% of an oscillation period.

The current-source bias circuit, also shown in Figure 2, dynamically adjusts the current through the simple nMOS current sources in the buffers so that current is held constant independent of supply voltage and common threshold shifts caused by substrate noise. The bias circuit uses a replica of half of the buffer stage combined with a single-stage differential amplifier compensated by the output load. The amplifier adjusts the current output of the nMOS current source so the voltage at the output of the replicated load element is equal to the control voltage (V_{CTRL}), as required for correct symmetric load swing limits. With no required swing reference voltage, the only bias voltage required is the control voltage itself. Although no device cascoding is used, the resultant static supply noise rejection is equivalent to that achievable by a buffer stage and a bias circuit with cascoding, without the necessity of the extra supply voltage.

The micrograph of the array oscillator is shown in Figure 4. Figure 5 and Figure 6 show the integral linearity and differential non-linearity versus position in the -22 mode measured from the output ports. The non-linearity in measured delays is caused by a bandwidth limitation in the output sense path. Table 1 summarizes the measured linearity for each mode from probe measurements directly on the array without using the output ports. The array signals are a factor of two more accurate than those obtained from the output ports. Figure 7 illustrates the frequency sensitivity to static supply voltage in the -12 mode. The measured static frequency rejection is less than 0.25% over most of the operating range for each mode, less than the 0.7% previously reported [2]. Table 2 summarizes the characteristics and performance of the array oscillator as a voltage-controlled oscillator for each mode.

Acknowledgments

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References

[1] Gasbarro, J., M. Horowitz, "A Single-Chip, Functional Tester for VLSI Circuits", ISSCC DIGEST OF TECHNICAL PAPERS, pp. 84-85, Feb. 1990.

[2] Young, I., et al., "A PLL Clock Generator with 5 to 110MHz Lock Range for Microprocessors", ISSCC DIGEST OF TECHNICAL PAPERS, pp. 50-51, Feb. 1992.

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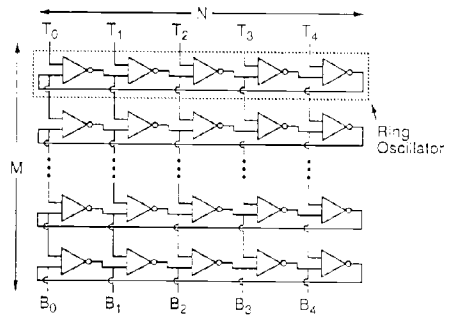

Figure 1: Array oscillator structure. All wires represent differential signal pairs.

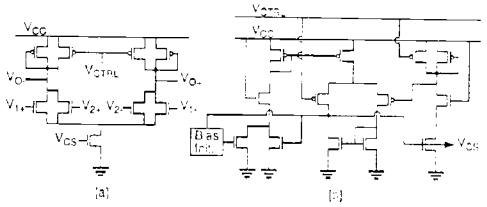

Figure 2: (a) Dual input differential buffer stage. (b) Current source bias circuit.

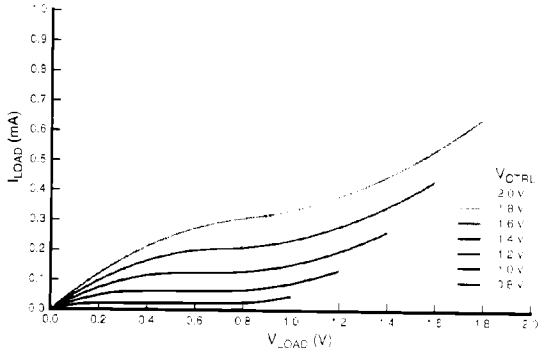

Figure 3: Simulated symmetric load I-V characteristics.

Figure 4: See page 273.

Frequency range, sensitivity	2-70MHz, 35MHz/V	(-22)
	5-135MHz, 74MHz/V	(-12)
	10-200MHz, 103MHz/V	(-2)
Static supply sensitivity:	0.25%/V @ 57MHz	(-12)
Minimum supply voltage:	2.5V @ 57MHz	(-12)
Power dissipation:	95mA* @ 57MHz	(-12)
Die area:	5.62mm²*	
Technology:	2μm n-well CMOS	

(*Array device sizes optimized for high-frequency operation.).

Table 2. Array oscillator characteristics as a VCO.

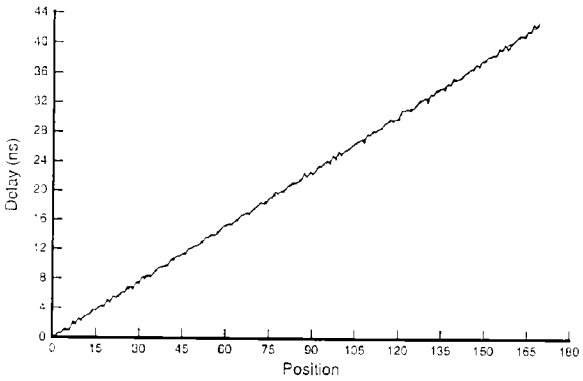

Figure 5: Integral linearity (23MHz, -22 mode).

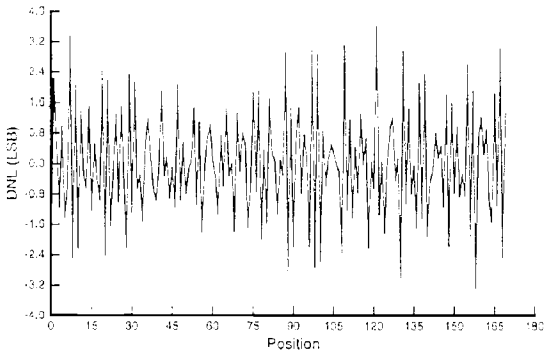

Figure 6: Differential non-linearity (23MHz, -22 mode).

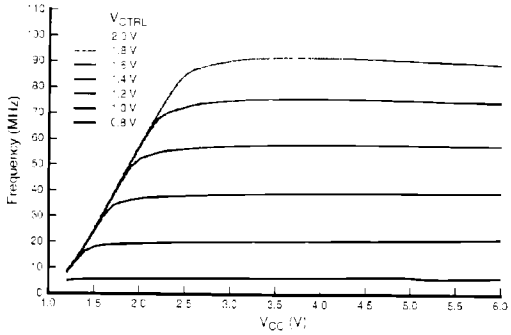

Figure 7: Frequency sensitivity to static supply voltage (-12 mode). At higher control voltages, chang ing die temperature causes a slight increase in frequency as the supply voltage is reduced.

Mode	-22	-12	-2
Frequency	25MHz	53MHz	87MHz
Resolution (1LSB)	238ps	112ps	68ps
RMS DNL	0.88LSB	0.99LSB	2.13LSB

Table 1. Array oscillator characteristics as precision delay generator (based on probe measurements directly on the array not at the output ports).

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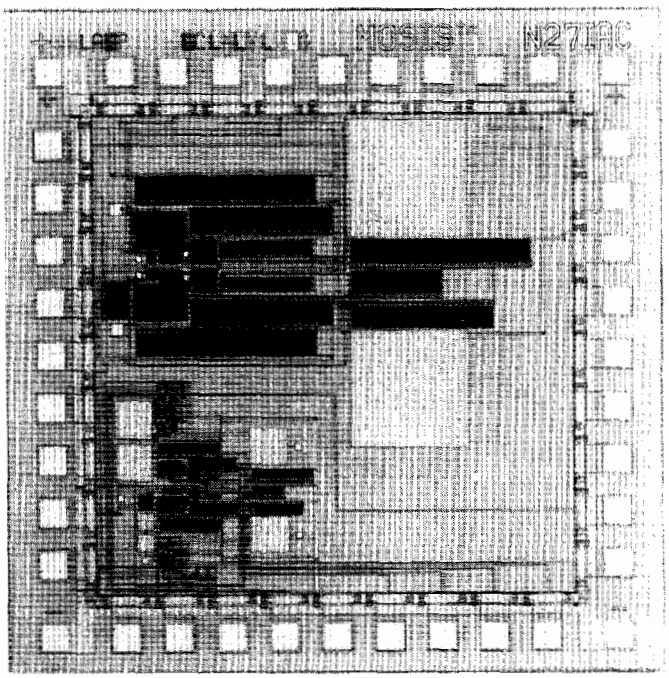

Figure 6: Die micrograph.

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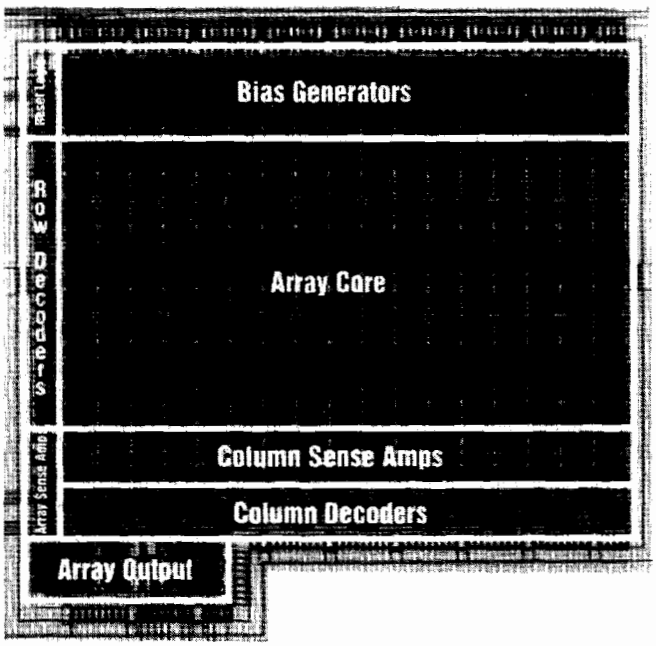

Figure 4: Die micrograph of array oscillator.