Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques

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Abstract— **Delay-locked loop (DLL) and phase-locked loop (PLL) designs based upon self-biased techniques are presented. The DLL and PLL designs achieve process technology independence, fixed damping factor, fixed bandwidth to operating frequency ratio, broad frequency range, input phase offset cancellation, and, most importantly, low input tracking jitter. Both the damping factor and the bandwidth to operating frequency ratio are determined completely by a ratio of capacitances. Self-biasing avoids the necessity for external biasing, which can require special bandgap bias circuits, by generating all of the internal bias voltages and currents from each other so that the bias levels are completely determined by the operating conditions. Fabricated in a 0.5-μm N-well CMOS gate array process, the PLL achieves an operating frequency range of 0.0025 MHz to 550 MHz and input tracking jitter of 384 ps at 250 MHz with 500 mV of low frequency square wave supply noise.**

I. Introduction

DELAY-LOCKED loops (DLL's) and phase-locked loops (PLL's) are often used in the I/O interfaces of digital integrated circuits in order to hide clock distribution delays and to improve overall system timing. In these applications, DLL's and PLL's must closely track the input clock. However, the rising demand for high-speed I/O has created an increasingly noisy environment in which DLL's and PLL's must function. This noise, typically in the form of supply and substrate noise, tends to cause the output clocks of DLL's and PLL's to jitter from their ideal timing. With a shrinking tolerance for jitter in the decreasing period of the output clock, the design of low jitter DLL's and PLL's has become very challenging.

Achieving low jitter in PLL and DLL designs can be difficult due to a number of design tradeoffs. Consider a typical PLL which is based on a voltage controlled oscillator (VCO). The amount of input tracking jitter produced as a result of supply and substrate noise is directly related to how quickly the PLL can correct the output frequency. To reduce the jitter, the loop bandwidth should be set as high as possible. Unfortunately, the loop bandwidth is affected by many process technology factors and is constrained to be well below the lowest operating frequency for stability [1]. These constraints can cause the PLL to have a narrow operating frequency range and poor jitter performance. Although a typical DLL is based on a delay line and thus simpler from a control perspective, it can have a limited delay range which leads to a set of problems similar to that of the PLL.

This paper describes both a DLL and PLL design based upon self-biased techniques [2]. Self-biasing can remove virtually all of the process technology and environmental variability that plagues PLL and DLL designs. Self-biasing can provide a bandwidth that tracks the operating frequency. This tracking bandwidth can in turn provide a very broad frequency range, minimized supply and substrate noise induced jitter with a high input tracking bandwidth, and, in general, very robust designs. Other benefits include a fixed damping factor for PLL's and input phase offset cancellation. Both the damping factor and the bandwidth to operating frequency ratio are determined completely by a ratio of capacitances giving effective process technology independence. The key idea behind self-biasing is that it allows circuits to choose the operating bias levels in which they function best. By referencing all bias voltages and currents to other generated bias voltages and currents, the operating bias levels are essentially established by the operating frequency. The need for external biasing, which can require special bandgap bias circuits, is completely avoided.

This paper will begin by reviewing a differential buffer stage design that provides high supply and substrate noise rejection and allows the possibility of self-biasing. The loop architecture for self-biased DLL and PLL designs will be presented in Section III and Section IV, respectively. A number of other loop components are critical to achieving low jitter in DLL and PLL designs. Section V will describe an improved phase-frequency comparator and differential-to-single-ended converter. The paper will also present some experimental results demonstrating the performance of the DLL and PLL designs.

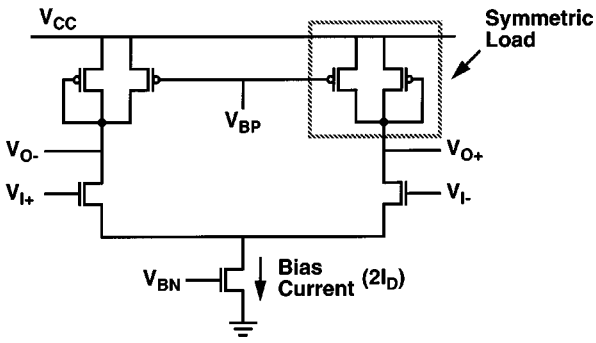

Fig. 1. Differential buffer delay stage with symmetric loads.

II. Differential Buffer Stage

In order to achieve low jitter operation, DLL and PLL designs require buffer stage designs with low supply and substrate noise sensitivity. The voltage-controlled delay line (VCDL) and the VCO used in the DLL and PLL designs are

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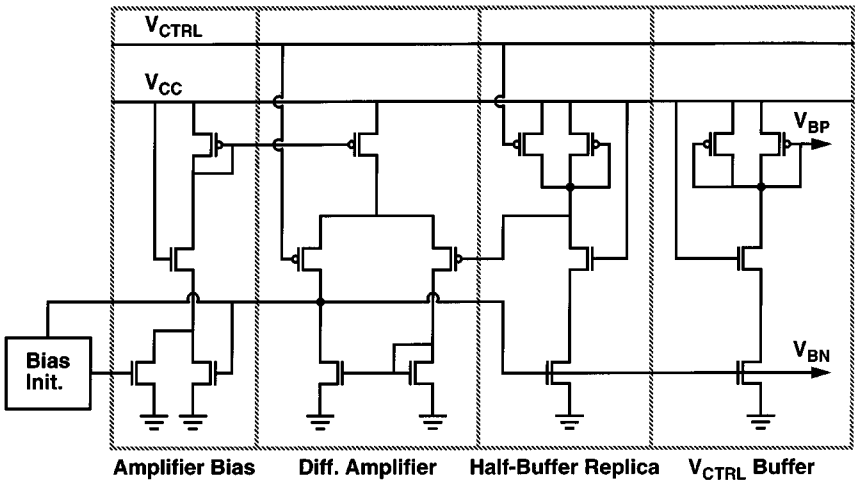

Fig. 2. Replica-feedback current source bias circuit.

based upon the differential buffer delay stages with symmetric loads and replica-feedback biasing [3].

The buffer stage, shown in Fig. 1, contains a source coupled pair with resistive load elements called symmetric loads. Symmetric loads consist of a diode-connected PMOS device in shunt with an equally sized biased PMOS device. The PMOS bias voltage V_{BP} is nominally equal to V_{CTRL}, the control input to the bias generator. Because of this equality, V_{CTRL} will be used instead of V_{BP} in subsequence references to the PMOS bias voltage. V_{CTRL} defines the lower voltage swing limit of the buffer outputs. The buffer delay changes with V_{CTRL} since the effective resistance of the load elements also changes with V_{CTRL}. It has been shown that these load elements lead to good control over delay and high dynamic supply noise rejection. The simple NMOS current source is dynamically biased with V_{BN} to compensate for drain and substrate voltage variations, achieving the effective performance of a cascode current source. However, this current source can provide high static supply and substrate noise rejection without the extra supply voltage required by cascode current sources.

The bias generator, shown in Fig. 2, produces the bias voltages V_{BN} and V_{BP} from V_{CTRL}. Its primary function is to continuously adjust the buffer bias current in order to provide the correct lower swing limit of V_{CTRL} for the buffer stages. In so doing, it establishes a current that is held constant and independent of supply voltage. It accomplishes this task by using a differential amplifier and a half-buffer replica. The amplifier adjusts V_{BN} so that the voltage at the output of the half-buffer replica is equal to V_{CTRL}, the lower swing limit. If the supply voltage changes, the amplifier will adjust to keep the swing and thus the bias current constant. The bandwidth of the bias generator is typically set equal to the operating frequency of the buffer stages so that the bias generator can track all supply and substrate voltage disturbances at frequencies that can affect the DLL and PLL designs. With this bias generator, the buffer stages have been shown to achieve a static supply noise rejection of about 0.25%/V while operating over a broad delay range with low supply voltage requirements that scale with the operating delay. The bias generator also provides a buffered version of V_{CTRL} at the V_{BP} output using an additional half-buffer replica. This output isolates V_{CTRL} from potential capacitive coupling in the buffer stages and plays an important role in the self-biased PLL design.

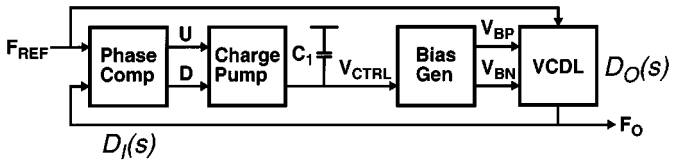

Fig. 3. Typical DLL block diagram (clock distribution omitted).

Buffer stages with low supply and substrate noise sensitivity are essential for low jitter DLL and PLL operation. With the foundation of a buffer stage design with low noise sensitivity, the next two sections will consider techniques for self-biasing DLL and PLL designs. Such techniques will provide further reductions in input tracking jitter by allowing the loop bandwidth to be set as close as possible to the operating frequency.

III. Self-Biased Delay-Locked Loop

A self-biased DLL is constructed by taking advantage of the control relationship offered by a typical DLL. A typical DLL is shown in Fig. 3. It is composed of a phase comparator, charge pump, loop filter, bias generator, and voltage controlled delay line. The negative feedback in the loop adjusts the delay through the VCDL by integrating the phase error that results between the periodic reference input and the delay line output. Once in lock, the VCDL will delay the reference input by a fixed amount to form the output such that there is no detected phase error between the reference and the output. The VCDL delay, therefore, must be a multiple of the reference input clock period. With the chip-wide clock distribution network included as part of the VCDL delay, the DLL can be used to rebuffer the input clock signal without adding any effective delay.

A. Closed-Loop Response

The frequency response of the DLL can be analyzed with a continuous time approximation, where the sampling operation

of the phase comparator is ignored. This approximation holds for bandwidths about a decade or more below the operating frequency. This bandwidth constraint is also required for stability due to the reduced phase margin near the higher order poles that result from the delay around the sampled feedback loop. Because the loop filter integrates the phase error, the DLL has a first-order closed loop response. The response could be formulated in terms of input phase and output phase. However, this set of variables is incompatible with a continuous time analysis since the sampled nature of the system would need to be considered. A better set of variables is input delay and output delay. The output delay is the delay between the reference input and the DLL output or, equivalently, the delay established by the VCDL. The input delay is the delay to which the phase comparator compares the output delay or, equivalently, the phase difference for which the phase comparator and charge pump generate no error signal. The output delay, $D_O(s)$, is related to the input delay, $D_I(s)$, by

$$D_O(s) = (D_I(s) - D_O(s)) \cdot F_{\mathrm{REF}} \cdot \frac{I_{CH}}{sC_1} \cdot K_{DL} \quad (1)$$

where F_{REF} is the reference frequency (Hz), I_{CH} is the charge pump current (A), C_1 is the loop filter capacitance (F), and K_{DL} is the VCDL gain (s/V). The product of the delay difference and the reference frequency is equal to the fraction of the reference period in which the charge pump is activated. The average charge pump output current is equal to this fraction times the peak charge pump current. The output delay is then equal to the product of the average charge pump current, the loop filter transfer function, and the delay line gain. The closed loop response is then given by

$$\frac{D_O(s)}{D_I(s)} = \frac{1}{1 + s/\omega_N} \quad (2)$$

where ω_N, defined as the loop bandwidth (rad/s), is given by

$$\omega_N = I_{CH} \cdot K_{DL} \cdot F_{\mathrm{REF}} \cdot \frac{1}{C_1}. \quad (3)$$

If the charge pump current I_{CH} and the VCDL gain K_{DL} are constant, the loop bandwidth ω_N will track the operating frequency ω_{REF}. However, the parameters I_{CH}, K_{DL}, and C_1 are process technology dependent and will cause the loop bandwidth to vary around the design target. In addition, constant gain VCDL's are typically implemented by interpolating between two closely delayed signals with a weighted sum which leads to a narrow delay range. Linear results are obtained only when the delay spacing is less than the signal edge rate. As the delay spacing increases, the interpolation becomes increasingly nonlinear. The delay range can be extended by using a VCDL with nonlinear delay control at the expense of a tracking loop bandwidth.

B. Bandwidth Tracking

Symmetric load buffer stages can be used to implement the VCDL in order to obtain a broad delay range. Fig. 4 shows their typical delay as a function of control voltage. The delay can change over a very broad range, but it is nonlinear with respect to the control voltage. In fact, the delay changes proportionally to $1/(V_{\mathrm{CTRL}} - V_T)$, with a slope K_{DL} proportional to $1/(V_{\mathrm{CTRL}} - V_T)^2$ or $1/I_D$, where I_D is one half of the buffer bias current.

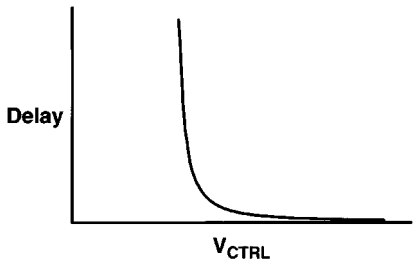

Fig. 4. Typical symmetric load buffer stage delay as a function of control voltage.

As the operating frequency is reduced, K_{DL} becomes larger, which increases the loop bandwidth relative to the operating frequency. This behavior is undesirable because the stability of the loop is undermined at lower frequencies, which in turn constrains the operating frequency range. Thus, even though nonlinear control over delay allows a VCDL to have a large delay range, stability constraints still lead to a small operating frequency range for the DLL.

The effect on stability for nonlinear control over delay can be corrected by applying self-biased techniques. Suppose that the charge pump current I_{CH} is set equal to the buffer bias current $2 \cdot I_D$. The $1/I_D$ dependence of K_{DL} can then be cancelled out leading to loop bandwidth that tracks the operating frequency without constraining the operating frequency range.

With this solution, the DLL design is completely self-biased as all bias voltages and currents are referenced to other generated bias voltages and currents. The bias generator generates all of the needed biases for the VCDL from V_{CTRL}, and the charge pump uses the current formed by V_{CTRL} to generate corrections to V_{CTRL}. The key difference from typical DLL designs is that no special bandgap bias circuit or the equivalent is needed to establish the charge pump current.

C. Quantitative Analysis

A more detailed analysis will show a very simple result for the relationship between the loop bandwidth and the operating frequency. First, a relationship between VCDL gain and control voltage is needed. Fig. 5 shows a symmetric load and its typical IV characteristics. The buffer bias current is $2 \cdot I_D$. It can be shown that the effective resistance of a symmetric load R_{EFF} is directly proportional to the small signal resistance at the ends of the swing range which is just one over the transconductance g_m for one of the two equally sized devices when biased at V_{BP} or, equivalently, V_{CTRL}. Thus, the buffer delay can be defined as

$$t = R_{\mathrm{EFF}} \cdot C_{\mathrm{EFF}} = \frac{1}{g_m} \cdot C_{\mathrm{EFF}} \quad (4)$$

where C_{EFF} is the effective buffer output capacitance.

Using a half-buffer replica, the bias generator sets the buffer bias current equal to the current through a symmetric load

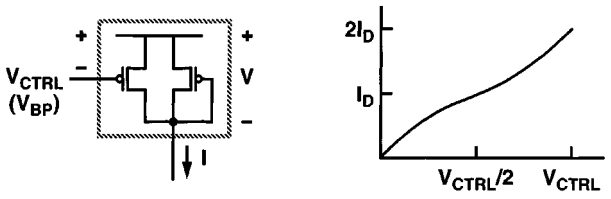

Fig. 5. Typical symmetric load IV characteristics.

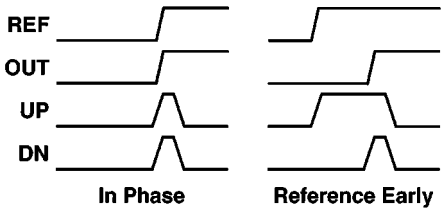

Fig. 6. Phase-frequency comparator waveforms with *UP* and *DN* asserted on every cycle.

with its output voltage at V_{CTRL}. In this case, the two equally sized PMOS devices are both biased at V_{CTRL} and each source half of the buffer bias current. Since these devices typically have greater than minimum channel length and are biased with moderate voltages, a simple quadratic model can be used for the drain current. The drain current for one of the two equally sized devices biased at V_{CTRL} is then given by

$$I_D = \frac{k}{2} \cdot (V_{\mathrm{CTRL}} - V_T)^2 \tag{5}$$

where k is the device transconductance of one of the PMOS devices. Taking the derivative with respect to V_{CTRL}, the transconductance is given by

$$g_m = k \cdot (V_{\mathrm{CTRL}} - V_T) = \sqrt{2 \cdot k \cdot I_D}. \tag{6}$$

The buffer delay is then given by

$$t = \frac{C_{\mathrm{EFF}}}{k \cdot (V_{CTRL} - V_T)}. \tag{7}$$

The delay for an n stage VCDL is given by

$$D = n \cdot t = \frac{C_B}{2 \cdot k \cdot (V_{\mathrm{CTRL}} - V_T)} \tag{8}$$

where C_B is defined as $2 \cdot n \cdot C_{\mathrm{EFF}}$ or, equivalently, the total buffer output capacitance for all stages. Taking the derivative with respect to V_{CTRL}, the VCDL gain is given by

$$\begin{aligned} K_{DL} &= \left| \frac{dD}{dV_{CTRL}} \right| = \frac{C_B}{2 \cdot k \cdot (V_{CTRL} - V_T)^2} \\ &= \frac{C_B}{4 \cdot I_D}. \end{aligned} \tag{9}$$

Thus, the gain is inversely proportional to buffer bias current.

With the relationship for K_{DL} established, the bandwidth to operating frequency ratio can be derived. Let the charge pump current be set to some multiple x of the buffer bias current such that

$$I_{CH} = x \cdot (2 \cdot I_D). \tag{10}$$

The bandwidth to operating frequency ratio is then given by

$$\begin{aligned} \frac{\omega_N}{\omega_{\mathrm{REF}}} &= \frac{1}{\omega_{\mathrm{REF}}} \cdot I_{CH} \cdot K_{DL} \cdot F_{\mathrm{REF}} \cdot \frac{1}{C_1} \\ &= \frac{1}{2\pi} \cdot I_{CH} \cdot K_{DL} \cdot \frac{1}{C_1} \\ &= \frac{1}{2\pi} \cdot x \cdot (2 \cdot I_D) \cdot \frac{C_B}{4 \cdot I_D} \cdot \frac{1}{C_1} \\ &= \frac{x}{4\pi} \cdot \frac{C_B}{C_1}. \end{aligned} \tag{11}$$

Thus, the bandwidth to operating frequency ratio is constant and completely determined by a ratio of capacitances that can be matched reasonably well in layout, dramatically reducing the process technology sensitivity of the design. In addition, the DLL can operate over the same broad frequency range achievable by a VCO based on the same buffer stages operating open loop.

D. Zero-Offset Charge Pump

The self-biased DLL design requires a charge pump current that will vary several decades over the operating frequency range. At low current levels, small charge offsets can lead to significant phase offsets. In addition, all phase comparators will typically assert their *UP* and *DN* outputs for equal durations on every cycle once the loop is in lock. In order to achieve zero static phase offset, the charge pump must transfer no net charge to the loop filter for these equal duration *UP* and *DN* pulses, which requires that the *UP* and *DN* currents be identical and independent of the charge pump output voltage.

An XOR phase comparator used for quadrature locking separately asserts its *UP* and *DN* outputs twice per cycle for equal durations. The same is true for a phase-frequency comparator (PFC) which is used for in-phase locking. In order to successfully avoid a dead-band region in the PFC as seen by the charge pump, the PFC must assert both *UP* and *DN* outputs on every cycle as shown in Fig. 6. A dead-band region is the range of input phase differences for which the PLL takes no corrective action. Such a dead-band region will result in additional input tracking jitter equal to the magnitude of the dead-band region. This requirement means that for in-phase inputs, the charge pump will see both its *UP* and *DN* inputs asserted for an equal and short period of time. If in-phase PFC inputs produce no *UP* or *DN* pulses, then it will take some finite phase difference before a large enough pulse is produced to turn on the charge pump, which leads to a dead-band region. If the reference is early with both *UP* and *DN* outputs asserted on every cycle, then the difference in duration between the *UP* and *DN* pulses will be equal to the input phase difference.

Self-biasing makes it possible to design a charge pump to have zero static phase offset when both the *UP* and *DN* outputs of the phase comparator are asserted for equal durations on every cycle with in-phase inputs. By constructing the charge pump from the symmetric load buffer stage, it can be guaranteed that the *UP* and *DN* currents for these equal duration pulses completely cancel out and transfer no net charge to the loop filter. A simplified schematic for the zero-offset charge pump is shown in Fig. 7. The charge

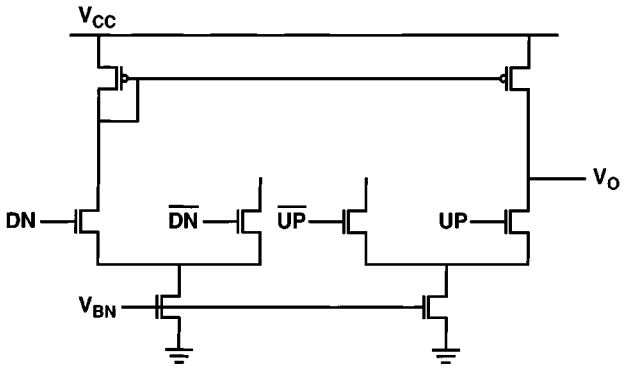

Fig. 7. Simplified schematic of the offset-cancelled charge pump.

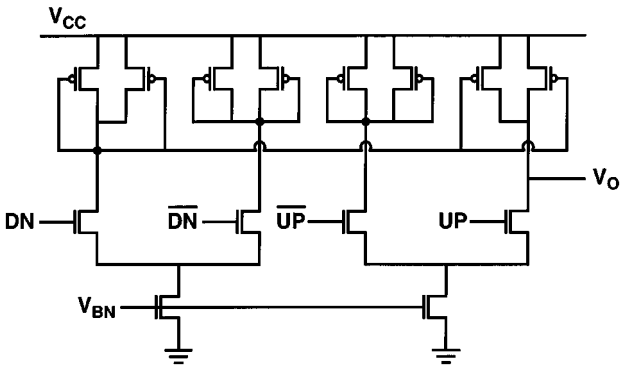

Fig. 8. Complete schematic of the offset-cancelled charge pump with symmetric loads.

pump is composed of two NMOS source coupled pairs each with a separate current source and connected by a current mirror made from symmetric load elements. Charge will be transferred from or to the loop filter connected to the output when the *UP* input or *DN* input, respectively, is switched high.

With both the *UP* and *DN* inputs asserted, the left source-coupled pair will behave like the half-buffer replica in the bias circuit and produce V_{CTRL} at the current mirror node. The PMOS device in the right source coupled pair will have V_{CTRL} at its gate and drain which is connected to the loop filter. This device will then source the exact same buffer bias current that is sunk by the remainder of the source coupled pair. With no net charge transferred to the loop filter, the charge pump will have zero static phase offset.

The complete schematic for the zero-offset charge pump is shown in Fig. 8. The current mirror is constructed from symmetric load elements. Also, the unselected source coupled pair outputs are connected to symmetric load elements to match the voltages at the other outputs. At this point, all of the elements necessary to construct a self-biased DLL have been considered. The following section shows that similar self-biasing techniques can be applied to a phase-locked loop.

IV. Self-Biased Phase-Locked Loop

A self-biased PLL, like the self-biased DLL, is constructed by taking advantage of the control relationship offered by a typical PLL. However, the control relationship and the additions to make it self-biased are more complicated than for the DLL. A typical PLL is shown in Fig. 9. It is composed of a phase comparator, charge pump, loop filter, bias generator, and VCO. The key differences from the DLL are that it uses a VCO instead of a delay line and that it requires a resistor in the loop filter for stability. The negative feedback in the loop adjusts the VCO output frequency by integrating the phase error that results between the periodic reference input and the divided VCO output. Once in lock, the VCO will generate an output with a frequency that is N times larger than that for the reference input such that there is no detected phase error between the reference and the divided output. With the chip-wide clock distribution network added in the feedback path to the divider, the PLL can be used to multiply and rebuffer an input clock signal without adding delay.

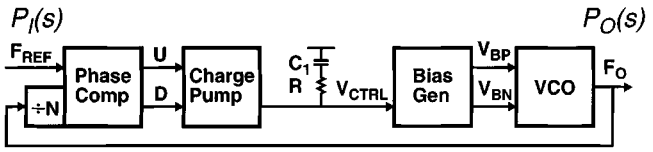

Fig. 9. Typical PLL block diagram (clock distribution omitted).

A. Closed-Loop Response

As with the DLL, the frequency response of the PLL can be analyzed with a continuous time approximation for bandwidths a decade or more below the operating frequency. This bandwidth constraint is also required for stability due to the reduced phase margin near the higher order poles that result from the delay around the sampled feedback loop. Because the loop filter integrates the charge representing the phase error and the VCO integrates the output frequency to form the output phase, the PLL has a second-order closed response. The output phase, $P_O(s)$, is related to the input phase, $P_I(s)$, by

$$P_O(s) = \left(P_I(s) - \frac{P_O(s)}{N}\right) \cdot I_{CH} \cdot \left(R + \frac{1}{sC_1}\right) \cdot K_V \cdot \frac{1}{s} \tag{12}$$

where I_{CH} is the charge pump current (A), R is the loop filter resistor (Ω), C_1 is the loop filter capacitance (F), and K_V is the VCO gain (Hz/V). The closed loop response is then given by

$$\begin{aligned}\frac{P_O(s)}{P_I(s)} &= \left(\frac{1}{N} + \frac{s}{I_{CH} \cdot (R + 1/(sC_1)) \cdot K_V}\right)^{-1} \\ &= \frac{N \cdot (1 + s \cdot C_1 \cdot R)}{1 + s \cdot C_1 \cdot R + s^2/(I_{CH}/C_1 \cdot K_V/N)}\end{aligned} \tag{13}$$

or, equivalently, by

$$\frac{P_O(s)}{P_I(s)} = N \cdot \frac{1 + 2 \cdot \zeta \cdot (s/\omega_N)}{1 + 2 \cdot \zeta \cdot (s/\omega_N) + (s/\omega_N)^2} \tag{14}$$

where ζ, defined as the damping factor, is given by

$$\zeta = \frac{1}{2} \cdot \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_V \cdot R^2 \cdot C_1} \tag{15}$$

and ω_N, defined as the loop bandwidth (rad/s), is given by

$$\omega_N = \frac{2 \cdot \zeta}{R \cdot C_1}. \tag{16}$$

The loop bandwidth and damping factor characterize the closed-loop response. The PLL is critically damped with a damping factor of one and overdamped with damping factors greater than one.

For a typical PLL, the charge pump current I_{CH}, VCO gain K_V, and loop filter resistance R are constant [4]. These conditions give rise to a constant damping factor and a constant loop bandwidth. A constant bandwidth can constrain the achievement of a wide operating frequency range and low input tracking jitter. A PLL adjusts its output frequency, not its output phase like a DLL. If the frequency is disturbed, the phase error that results from each cycle of the disturbance will accumulate for many cycles until the loop can correct the frequency error. The error will be accumulated for a number of cycles proportional to the operating frequency divided by the loop bandwidth. Thus, ω_N should be positioned as close as possible to ω_{REF} to minimize the total phase error. In addition, ω_N depends on I_{CH}, K_V, R, and C_1, but not on ω_{REF}. All of these parameters have independent variability. However, ω_N must be a decade below the lowest operating frequency for stability. The result is that ω_N must be conservatively set for stability at the lowest operating frequency with worst case process variations, rather than set for optimized jitter performance.

B. Bandwidth Tracking

Ideally, both ζ and $\omega_N/\omega_{\mathrm{REF}}$ should be constant so that there is no limit on the operating frequency range and so that the jitter performance can be improved. I_{CH} could be set equal to the buffer bias current $2{\cdot}I_D$ as done in self-biasing the DLL, but this is not sufficient since ζ would change with operating frequency as a result of a square root of I_D dependence. To keep ζ constant with operating frequency, two parameters, such as I_{CH} and R, must vary. I_{CH} can be set equal to the buffer bias current and R can be set to vary inversely proportionally to the square root of the buffer bias current. ζ will then remain constant, but ω_N will be proportional to the square root of the buffer bias current.

To obtain a tracking bandwidth, the VCO operating frequency should have the same dependency on the buffer bias current as the loop bandwidth ω_N. Symmetric load buffer stages can be used to implement the VCO in order to obtain a broad frequency range. Fig. 10 shows their typical frequency as a function of control voltage. The frequency is proportional to $V_{\mathrm{CTRL}} - V_T$ or, equivalently, the square root of I_D, and the slope is constant. Thus, K_V is constant and the reference frequency ω_{REF} is proportional to the square root of the buffer bias current. Since both ω_N and ω_{REF} are proportional to the square root of the buffer bias current, the loop bandwidth will track the operating frequency.

C. Feed-Forward Zero

It may seem difficult to obtain a resistor for the loop filter that varies inversely proportionally to the square root of the buffer bias current. However, this resistor can be formed from the small-signal resistance $1/g_m$ for a diode-connected device, where g_m is proportional to the square root of the buffer bias current. The integration of such a resistance into the loop filter can be accomplished by applying a transformation to the loop filter as illustrated in Fig. 11.

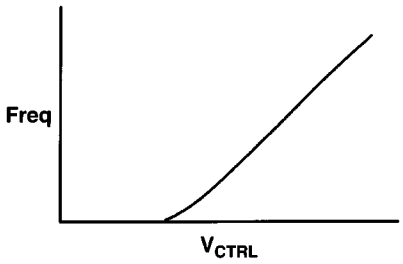

Fig. 10. Typical VCO frequency as a function of control voltage when implemented with symmetric load buffer stages.

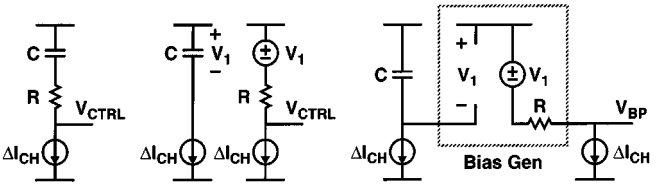

Fig. 11. Transformation of the loop filter for the integration of the loop filter resistor.

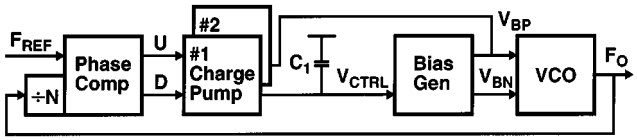

Fig. 12. Complete self-biased PLL block diagram (clock distribution omitted).

The loop filter for a PLL is typically a capacitor in series with a resistor that is driven by the charge pump current ΔI_{CH}. The control voltage is then the sum of the voltage drops across the capacitor and resistor. The voltage drops across the capacitor and resistor can be generated separately, as long as the same charge pump current is applied to each of them. The two voltage drops can then be summed to form the control voltage by replicating the voltage across the capacitor with a voltage source placed in series with the resistor.

It just so happens that the bias generator can conveniently implement this voltage source and resistor since it buffers V_{CTRL} to form V_{BP} with a finite output resistance. Referring back to the buffer bias circuit in Fig. 2, it is evident that this resistance is established by a diode-connected symmetric load or, equivalently, a diode-connected PMOS device. Thus, the resistance is equal to $1/g_m$ or inversely proportional to the square root of the buffer bias current. Thus, the self-biased PLL can be completed simply by adding an additional charge pump current [5] to the bias generator's V_{BP} output as shown in Fig. 12. Therefore, as with the DLL, this PLL design is completely self-biased.

D. Quantitative Analysis

As for the DLL, a more detailed analysis will show a very simple result for the damping factor and the relationship

between the loop bandwidth and the operating frequency. First, a relationship between VCO gain and control voltage is needed. The oscillation frequency for an n-stage VCO is given by

$$F = \frac{1}{2 \cdot n \cdot t} = \frac{k \cdot (V_{\mathrm{CTRL}} - V_T)}{C_B} = \frac{\sqrt{2 \cdot k \cdot I_D}}{C_B} \tag{17}$$

where C_B is once again defined as $2 \cdot n \cdot C_{\mathrm{EFF}}$. Thus, the oscillation frequency is proportional to the square root of the buffer bias current. Taking the derivative with respect to V_{CTRL}, the VCO gain K_V is given by

$$K_V = \left| \frac{dF}{dV_{\mathrm{CTRL}}} \right| = \frac{k}{C_B} \tag{18}$$

which is independent of the buffer bias current.

With the relationship for K_V established, the damping factor and bandwidth to operating frequency ratio can be derived. Let the charge pump current be set to some multiple x of the buffer bias current such that

$$I_{CH} = x \cdot (2 \cdot I_D). \tag{19}$$

Also, let the diode-connected symmetric load in the bias generator that establishes the loop filter resistance be y times larger than the symmetric loads used in the buffer stages such that

$$R = \frac{y}{2 \cdot g_m} = \frac{y}{\sqrt{8 \cdot k \cdot I_D}}. \tag{20}$$

Substituting in the expressions for I_{CH}, K_V, and R, the damping factor is then given by

$$\begin{aligned} \zeta &= \frac{1}{2} \cdot \sqrt{\frac{1}{N} \cdot I_{CH} \cdot K_V \cdot R^2 \cdot C_1} \\ &= \frac{1}{2} \cdot \sqrt{\frac{1}{N} \cdot x \cdot (2 \cdot I_D) \cdot \frac{k}{C_B} \cdot \frac{y^2}{8 \cdot k \cdot I_D} \cdot C_1} \\ &= \frac{y}{4} \cdot \sqrt{\frac{x}{N}} \cdot \sqrt{\frac{C_1}{C_B}}. \end{aligned} \tag{21}$$

Thus, the damping factor is simply a constant times the square root of the ratio of two capacitances. Substituting in the expressions for ζ, R, and F_{REF}, the loop bandwidth to operating frequency ratio is given by

$$\begin{aligned} \frac{\omega_N}{\omega_{\mathrm{REF}}} &= \frac{1}{2\pi \cdot F_{\mathrm{REF}}} \cdot \frac{2 \cdot \zeta}{R \cdot C_1} \\ &= \frac{1}{2\pi} \cdot \frac{N \cdot C_B}{\sqrt{2 \cdot k \cdot I_D}} \cdot \frac{y}{4} \cdot \sqrt{\frac{x}{N}} \cdot \sqrt{\frac{C_1}{C_B}} \\ &\quad \cdot \frac{\sqrt{8 \cdot k \cdot I_D}}{y} \cdot \frac{2}{C_1} \\ &= \frac{x \cdot N}{2\pi} \cdot \sqrt{\frac{C_B}{C_1}}. \end{aligned} \tag{22}$$

The loop bandwidth to operating frequency ratio is also a constant times the square root of the ratio of the same two capacitances.

Thus, the loop bandwidth will track operating frequency and, therefore, sets no constraint on the operating frequency range. The PLL can operate over the same broad frequency range achievable by the VCO operating open loop. The only process technology dependence is on a ratio of capacitances that can be matched reasonably well in layout. ω_N and ζ can be aggressively set to minimize jitter accumulation over all operating frequencies.

E. PLL Capture Behavior

A useful artifact of the self-biasing used in the PLL is a nonlinear capture behavior. Typical PLL's will slew toward the final target frequency at roughly a constant rate. A phase-frequency comparator will detect on average a phase error of a half cycle which will cause the charge pump to source or sink on average half of its charge pump current to the loop filter. The resulting change in control voltage is given by

$$\left| \frac{dV_{\mathrm{CTRL}}}{dt} \right| = \frac{1}{2} \cdot \frac{1}{C_1} \cdot I_{CH} \tag{23}$$

which leads to the result

$$V_{\mathrm{CTRL}}(t) = V_{\mathrm{CTRL}}(0) \pm \frac{1}{2 \cdot C_1} \cdot I_{CH} \cdot t \tag{24}$$

and

$$t = |V_{\mathrm{CTRL}}(t) - V_{\mathrm{CTRL}}(0)| \cdot \frac{2 \cdot C_1}{I_{CH}}. \tag{25}$$

For the self-biased PLL, the charge pump current, which is proportional to the buffer bias current, changes with the control voltage and the VCO output frequency. This dependency means that the rate of change in the control voltage or the VCO output frequency will increase when approaching higher frequencies and decrease when approaching lower frequencies. The resulting change in control voltage is given by

$$\left| \frac{dV_{\mathrm{CTRL}}}{dt} \right| = \frac{1}{2} \cdot \frac{1}{C_1} \cdot I_{CH} = \frac{x \cdot k}{4 \cdot C_1} \cdot (V_{\mathrm{CTRL}} - V_T)^2 \tag{26}$$

which leads to the result

$$V_{\mathrm{CTRL}}(t) = \left(\frac{1}{V_{\mathrm{CTRL}}(0) - V_T} \pm \frac{x \cdot k \cdot t}{4 \cdot C_1} \right)^{-1} + V_T \tag{27}$$

and

$$t = \frac{4 \cdot C_1}{x \cdot k} \cdot \left| \frac{1}{V_{\mathrm{CTRL}}(0) - V_T} - \frac{1}{V_{\mathrm{CTRL}}(t) - V_T} \right|. \tag{28}$$

The control voltage as a function of time during capture is plotted in Fig. 13. The result is that the self-biased PLL will slew toward lock at the fastest rate possible using the maximum charge pump current such that the instantaneous loop bandwidth does not exceed that required to lock at the current VCO output frequency. In contrast, a typical PLL will only be able to slew toward lock at a constant rate using a fixed charge pump current such that the loop bandwidth does not exceed that required to lock at the lowest operating frequency of interest. Thus, the self-biased PLL will exhibit much faster locking times when locking from similar or higher operating frequencies. If, however, the self-biased PLL is started at a very low operating frequency, possibly in the low kilohertz range, it will exhibit very slow locking times.

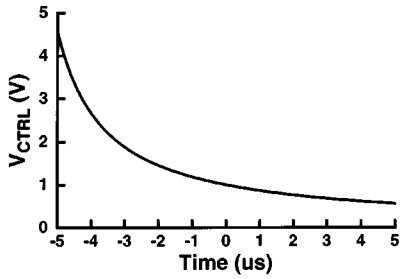

Fig. 13. Self-biased PLL control voltage as a function of time during capture.

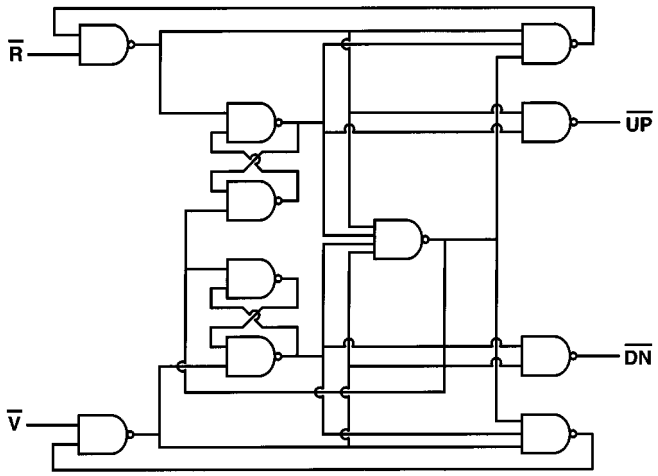

Fig. 14. Phase-frequency comparator with equal short duration output pulses for in-phase inputs.

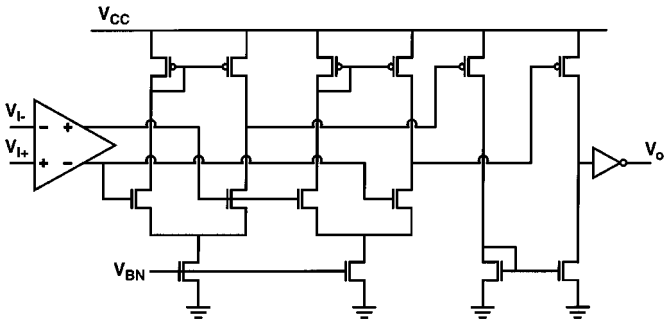

Fig. 15. Differential-to-single-ended converter with 50% duty cycle output.

V. Additional Loop Components

In completing the self-biased DLL and PLL designs, some additional loop components are required. These include a phase-frequency comparator and a differential-to-single-ended converter. Although they are not essential to the self-biased techniques, they are important to the overall performance of the self-biased DLL and PLL designs.

A. Phase-Frequency Comparator

Equal and short duration pulses at the *UP* and *DN* outputs of the PFC are needed for in-phase inputs in order to eliminate a dead-band in the PFC as seen by the charge pump. Such a dead-band will lead to additional input tracking jitter, as discussed in Section III-D. In order to guarantee equal and short duration pulses, some delay is typically added in the reset path. Because of this added delay, a signal transition at the R or V input will cause the corresponding *UP* or *DN* output to be asserted for some short delay before both outputs are reset for the case when the other output was already asserted. However, adding delay in the reset path can reduce the maximum operating frequency of the PFC. The maximum operating frequency is determined by the amount of time required to reset the PFC after receiving the last set of input transitions so that it is ready to detect the next set of input transitions. The phase-frequency comparator shown in Fig. 14, based on a conventional PFC [4], instead adds delay only in the output reset path by forming the outputs without including the reset signal generated by the four input NAND gate. Rather than obtaining the outputs from the three input NAND gates at the far right, the outputs are obtained from copies of the gates with the reset signal input deleted. The outputs are still reset, but through a slower path that includes the two NAND gates which form the SR latches. Since the input reset path is unchanged, the maximum operating frequency is unaffected.

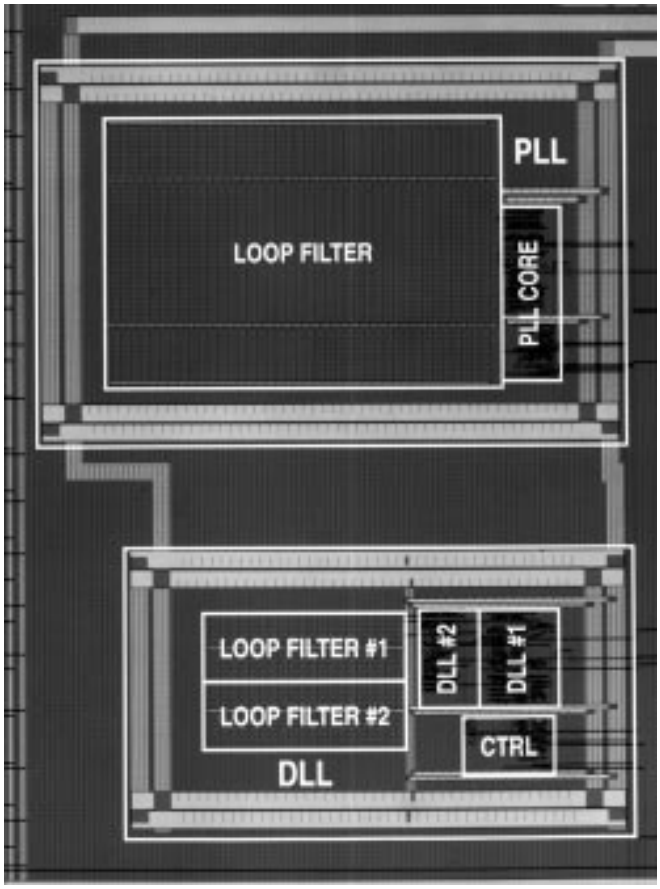

Fig. 16. Die micrograph of the dual-loop DLL and PLL.

B. Differential-to-Single-Ended Converter

PLL's are typically designed to operate at twice the chip operating frequency so that their outputs can be divided by two in order to guarantee a 50% duty cycle [4]. This practice is particularly wasteful if the delay elements generate differential signals. The maximum operating frequency will be reduced

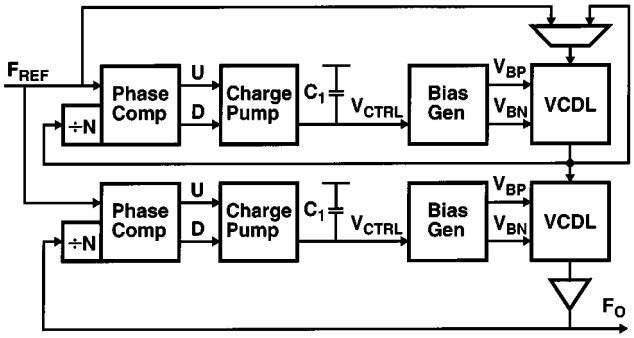

Fig. 17. Dual-loop DLL block diagram.

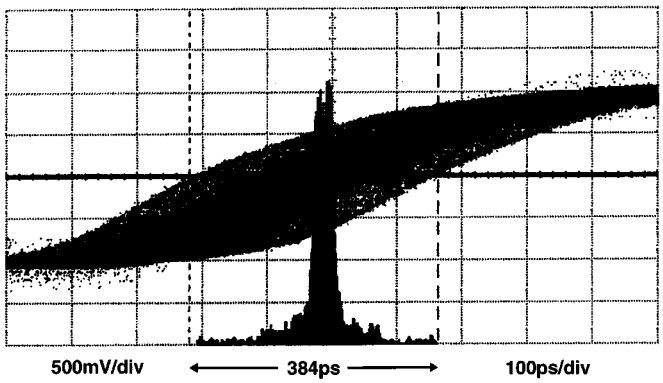

Fig. 18. Measured PLL tracking jitter with 500 mV of supply noise.

by a factor of two and the input tracking jitter performance can be adversely affected. The requirement for a 50% duty cycle can be satisfied without operating the PLL at twice the chip operating frequency if a single-ended output with 50% duty cycle can be obtained from the differential output signal. The differential-to-single-ended converter circuit shown in Fig. 15 can produce such a 50% duty cycle output. It is composed of two opposite phase NMOS differential amplifiers driving two PMOS common-source amplifiers connected by an NMOS current mirror. The two NMOS differential amplifiers are constructed from symmetric load buffer stages using the same NMOS current source bias voltage as the driving buffer stages so that they receive the correct common-mode input voltage level. They provide signal amplification and a dc bias point for the PMOS common-source amplifiers. The PMOS common-source amplifiers provide additional signal amplification and conversion to a single-ended output through the NMOS current mirror. Because the two levels of amplification are differentially balanced with a wide bandwidth, the opposing differential input transitions have equal delay to the output. The limitations of this circuit in converting the differential signal transitions into rising and falling single-ended output transitions at medium and high bias levels are identical to those of a divider in converting single direction transitions into rising and falling single-ended output transitions. However, using this circuit instead of a divider to generate a 50% duty cycle output can substantially relax the design constraints on the VCO for high frequency designs.

VI. Experimental Results

Both the self-biased DLL and PLL designs were fabricated in a 0.5-μm N-well CMOS gate array process. A micrograph of the fabricated designs with a superimposed floor plan is shown in Fig. 16. The loop filter capacitors for both the DLL and PLL are integrated on-chip using PMOS gate array devices. The capacitor arrays also contain an equal number of NMOS devices that are in rows interleaved between the PMOS devices. These NMOS devices are used to make a supply bypass capacitor. The DLL design actually implemented was a dual-loop DLL design [2], [6], as shown in Fig. 17, which contains two cascaded DLL's to allow it to perform frequency multiplication and duty cycle adjustment.

The PLL input-to-output tracking jitter performance with 500 mV of 1 MHz square wave supply noise is illustrated in Fig. 18. This square wave supply noise has edge transition times less than 10 ns. It is important to note that low frequency square wave supply noise is one of the most extreme jitter tests that can be performed on a PLL. Sine wave supply noise at the loop bandwidth typically leads to much less jitter. The confined central peaks indicate very low static phase offset sensitivity to supply voltage.

TABLE I
Dual-Loop DLL Performance Characteristics Measured at 250 MHz with 500 mV of 1 MHz Square Wave Supply Noise

Operating frequency range:	0.0025 MHz–400 MHz @ 3.3 V
Minimum supply requirements:	2.45 V, 8.6 mA
Input offset, sensitivity:	112 ps, <100 ps/100 MHz
Tracking jitter, sensitivity:	610 ps, 1165 ps/V (P-P)
Cycle-to-cycle jitter, sensitivity:	262 ps, 430 ps/V (P-P)
Block area:	1.18 mm^2
Technology:	0.5-μm N-well CMOS gate array

TABLE II
PLL Performance Characteristics Measured at 250 MHz with 500 mV of 1 MHz Square Wave Supply Noise

Operating frequency range:	0.0025 MHz–550 MHz @ 3.3 V
Minimum supply requirements:	2.10 V, 4.4 mA
Input offset, sensitivity:	<25 ps, <10 ps/100 MHz
Tracking jitter, sensitivity:	384 ps, 704 ps/V (P-P)
Cycle-to-cycle jitter, sensitivity:	144 ps, 290 ps/V (P-P)
Block area:	1.91 mm^2
Technology:	0.5-μm N-well CMOS gate array

Performance characteristics of the dual-loop DLL and PLL are summarized in Table I and Table II, respectively. Both designs have a frequency range spanning five orders of magnitude. This large range should allow a single design to satisfy a variety of operating frequency requirements. The cycle-to-cycle jitter listed is the jitter in the period of the output. The measured jitter, although small, was increased by the gate array implementation of the loop filter capacitors which contain the interleaved rows of unrelated NMOS devices that lead to control voltage coupling to ground. The die area for the dual-loop DLL and PLL was substantially increased by the inefficient implementation of the loop filter capacitors. With custom silicon, the PLL only occupies 0.4 mm^2.

The PLL design performed about 50% better than the dual-loop DLL design. This difference in performance may have resulted from larger capacitive coupling to the DLL loop filter

capacitors since they were eight times smaller than the PLL loop filter capacitor.

VII. Conclusions

Self-biasing greatly simplifies DLL and PLL designs. It eliminates the need for precise currents, eliminates virtually all process technology dependencies, and makes a wide operating frequency range possible. The bandwidth to operating frequency ratio and the PLL damping factor are fixed completely by a ratio of capacitances. The operating frequency range is limited only by the buffer stage design. Self-biasing facilitates the construction of an input offset-cancelled charge pump. Self-biasing also allows a PLL to have the largest possible loop bandwidth over all operating frequencies for minimal jitter accumulation. The phase-frequency comparator design provides equal short duration output pulses for in-phase inputs without reducing its maximum operating frequency. The differential-to-single-ended converter can convert differential input signals into single-ended output signals with 50% duty cycle, avoiding the need for dividing by two. Fabricated in a 0.5-μm N-well CMOS gate array process, the PLL achieves an operating frequency range of 0.0025 MHz to 550 MHz and input tracking jitter of 384 ps at 250 MHz with 500 mV of low frequency square wave supply noise.

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Dr. Maneatis is a member of Tau Beta Pi, Eta Kappa Nu, and Phi Beta Kappa and a Registered Professional Electrical Engineer in the State of California.